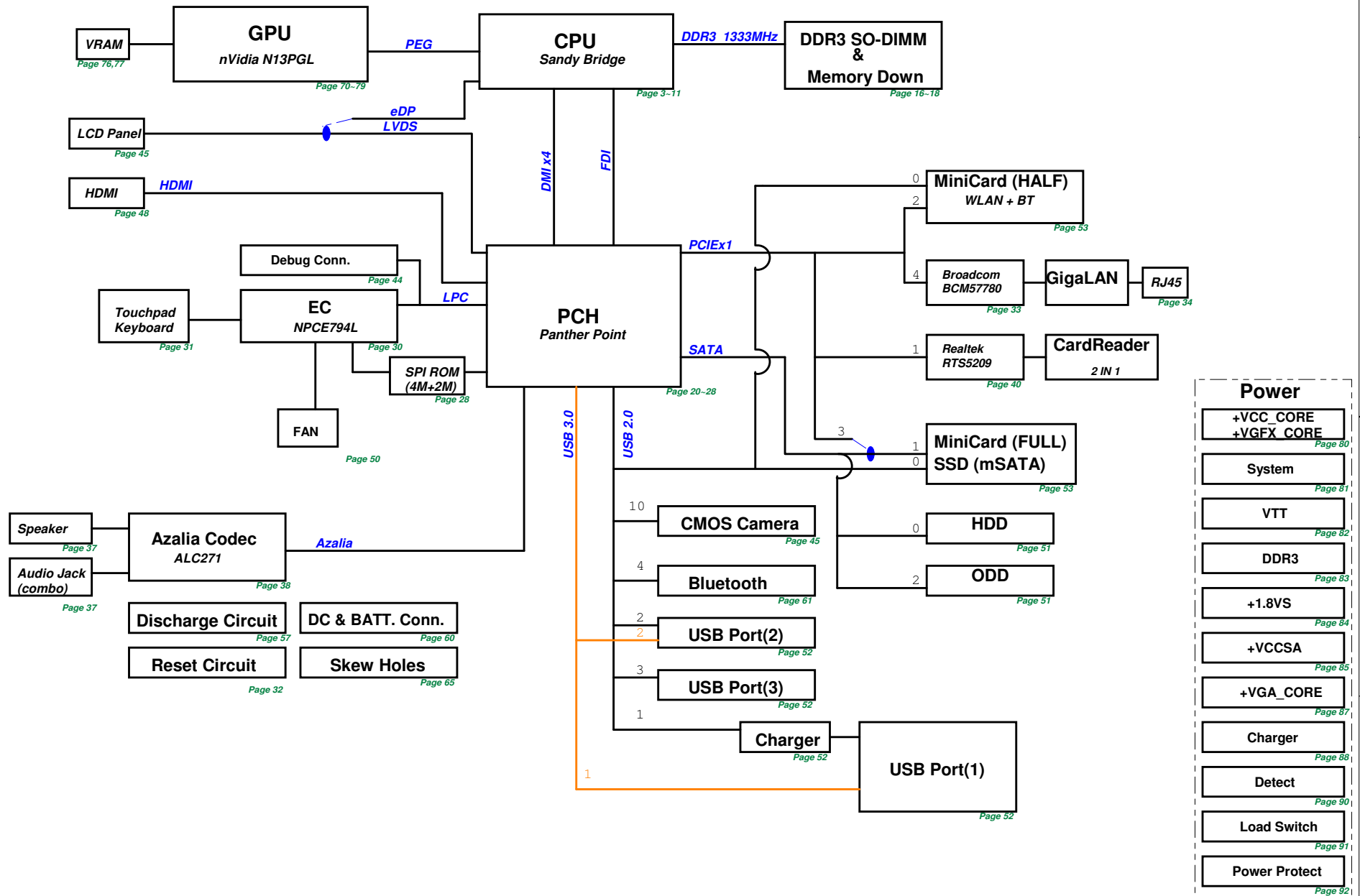


JM50 Ultrabook Block Diagram Rev 1.0



PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

WWW.AliSaler.Com

EC
NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

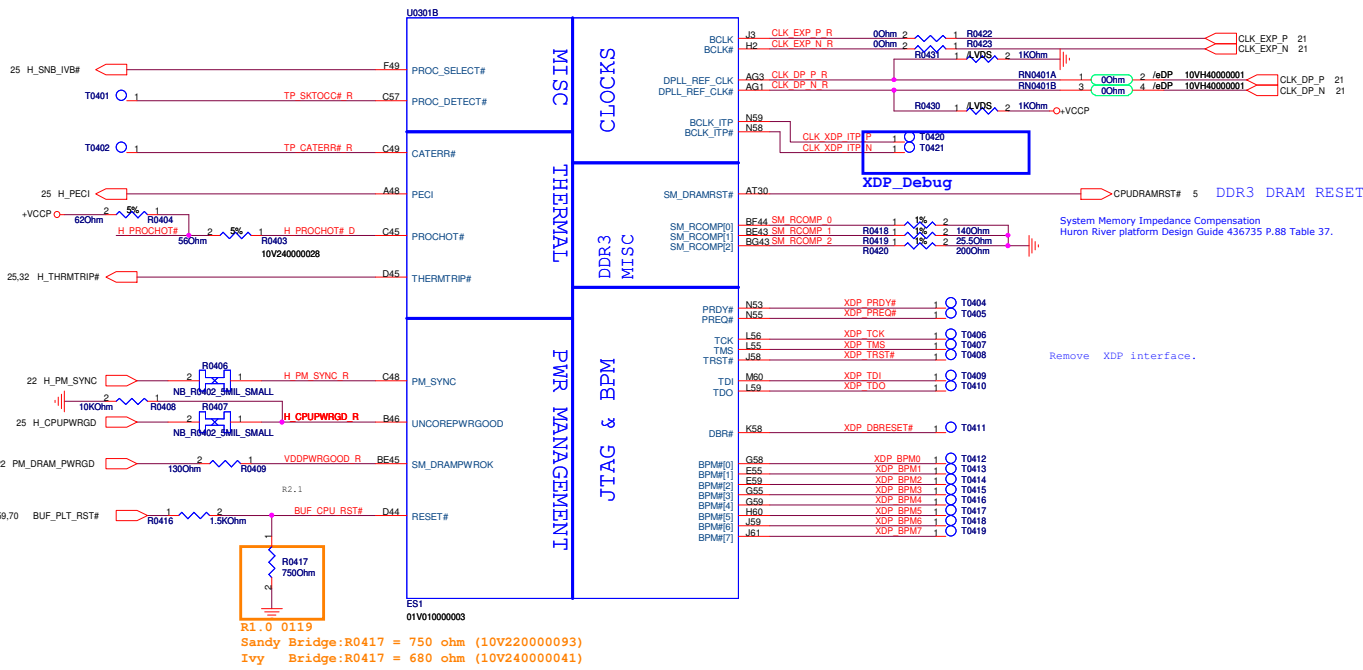
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A



+1.5VS_VCCDDQ 7

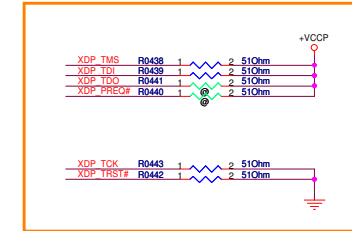
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+3VSUS 22,24,28,30,60,81,92

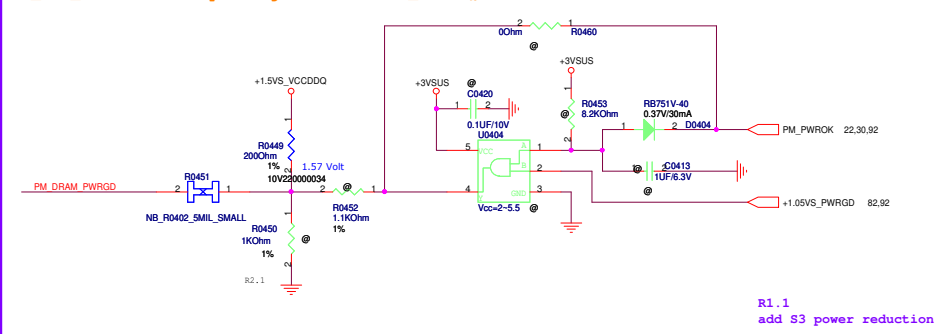
+VCCP 3,6,7,30,32,57,82

+3V 24,45,57,59,61,91

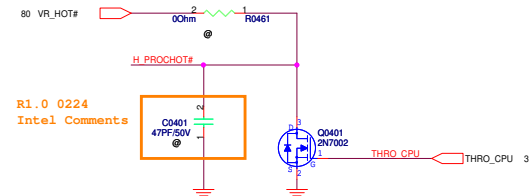
R.10 PU/PD for JTAG signals

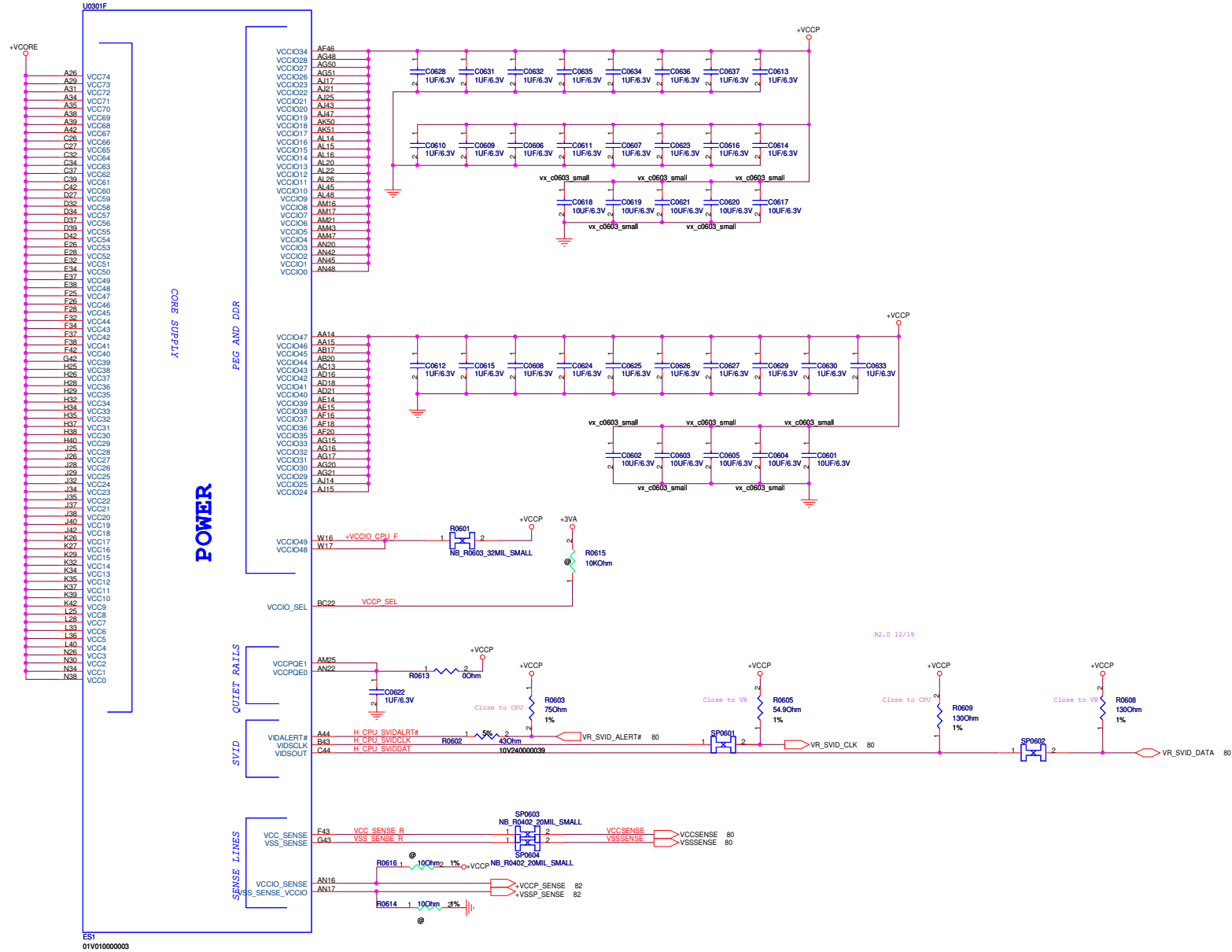


PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ Different from EVEREST










- If support S3 power reduction with power good.
1. Mount U0404, D0404, C0413, C0420, R0450, R0452, R0453, Unmount R0460
 2. Change R0449 to 1kohm from 200ohm, change R0409 to 0ohm from 130ohm - Design Guide 1.0 page 106





+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VCCP		+VCCP	3,4,6,30,32,57,82
+1.5V		+1.5V	5,16,17,18,57,60,63
+VCCSA		+VCCSA	85
+1.8VS		+1.8VS	25,26,57,80,84
+VGFX_CORE		+VGFX_CORE	9,80
+1.5VS		+1.5VS	26,53,57,91
+V_SM_VREF		+V_SM_VREF	83

The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It begins with a 5V input from a USB core, which is connected to a series of capacitors (C0725 to C0728, C0717 to C0722) and a voltage regulator (vx_c0603_small). The output of the regulator is 1.52V, which is then connected to a series of capacitors (C0790 to C0796, C0738 to C0745) and a final output filter capacitor (C0746).

U3031G	
A4A6	VAXG2
A4B7	VAXG2
A4B50	VAXG1
A4B51	VAXG1
A4B52	VAXG1
A4B53	VAXG1
A4B54	VAXG1
A4B56	VAXG1
A4B58	VAXG1
A4B59	VAXG1
C681	VAXG1
D048	VAXG1
D050	VAXG9
D051	VAXG7
D052	VAXG6
D053	VAXG6
D055	VAXG4
D056	VAXG4
D058	VAXG2
D059	VAXG1
E4E6	VAXG0
N45	VAXG5
P48	VAXG5
P50	VAXG5
P51	VAXG5
P52	VAXG5
P53	VAXG4
P54	VAXG4
P55	VAXG4
P61	VAXG4
T48	VAXG4
T58	VAXG4
T61	VAXG4
U46	VAXG4
V47	VAXG4
V48	VAXG3
V50	VAXG3
V51	VAXG3
V52	VAXG3
V53	VAXG3
V55	VAXG3
V56	VAXG3
V58	VAXG3
V59	VAXG3
W50	VAXG2
W51	VAXG2
W52	VAXG2
W53	VAXG2
W55	VAXG2
W56	VAXG2
W61	VAXG2
Y48	VAXG2

POWER

GRAPHICS

DDR3 - 1.5V RAILS

[illegible]

$\Gamma_{+V_SM_REF} 10mil$

MCM V05

+1.5VS V

```
R1.1
add S3 power reduction
```

MAX: 5A

Chief River

Decoupling guide from Intel (EE)

- +1.5VS_VCCDDQ
- 1uF * 10pcs
- 10uF * 8pcs
- 330uF * 1pcs

Processor I/O supply
voltage for DDR3
(DC + AC specification)

VDDQ 5A

PLL supply voltage
(DC + AC specification)

+1.8VS

Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

Filtered(BGA Only)

+1.5VS_VCCDDQ

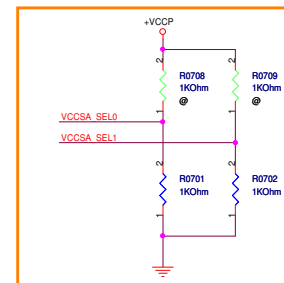
00hm

Chief River

R2.2, 03/05

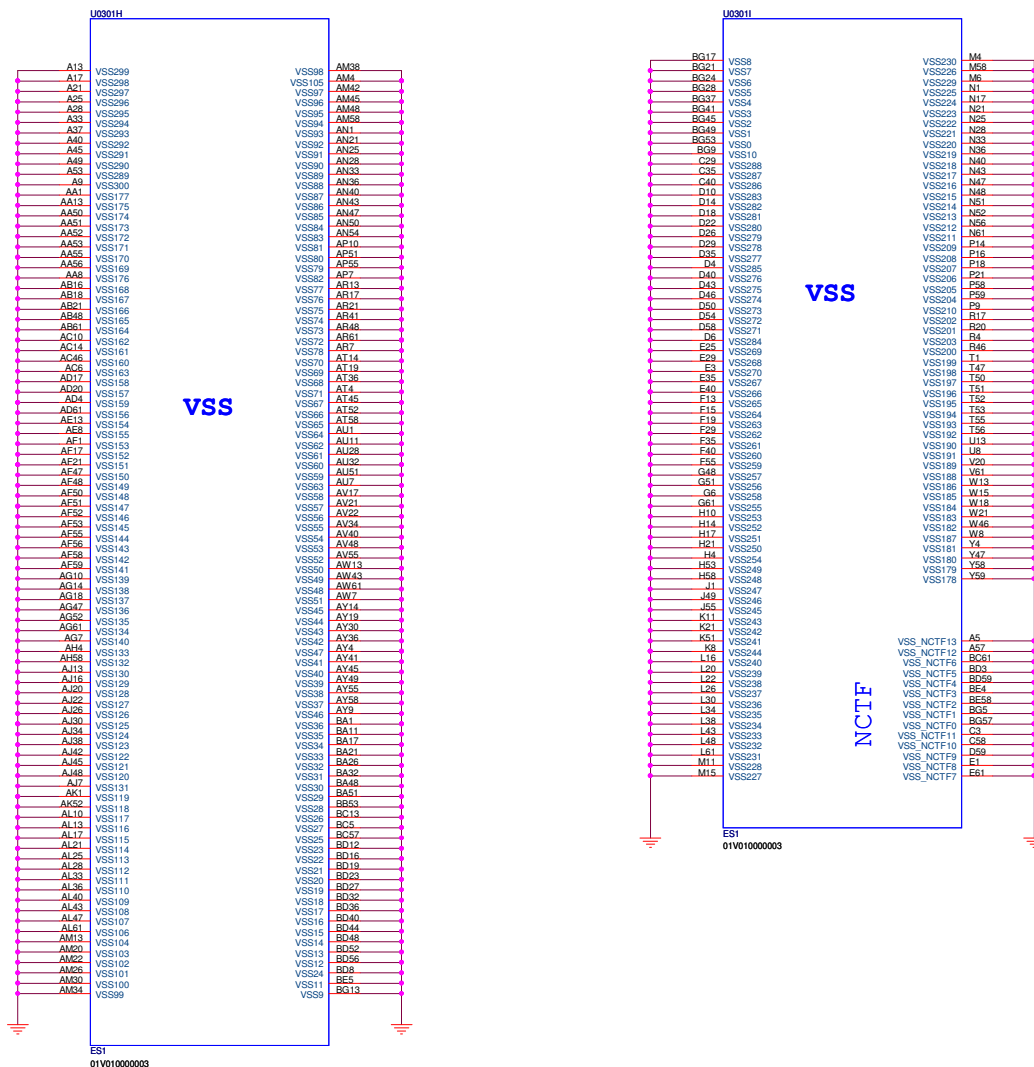
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

R1.0 0209
Intel Comments

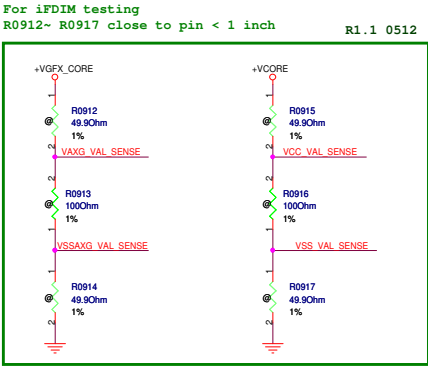
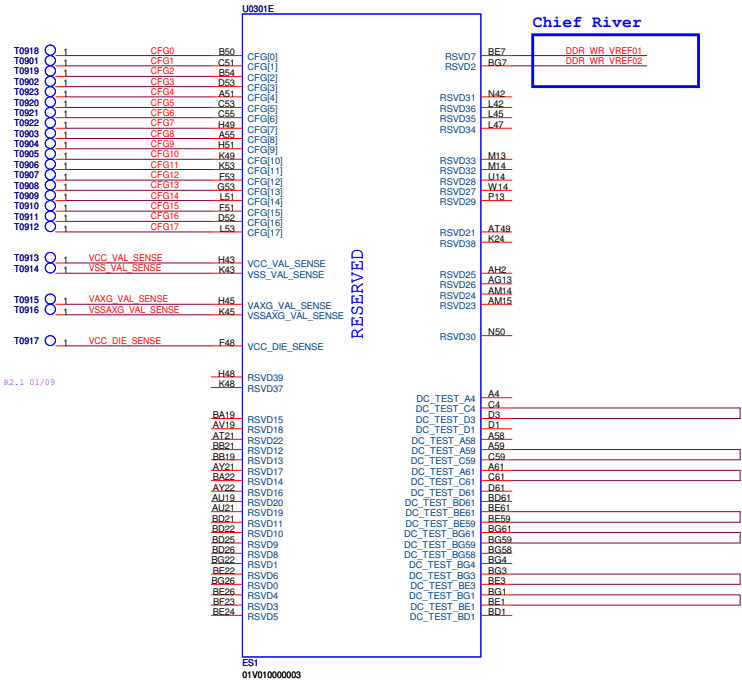
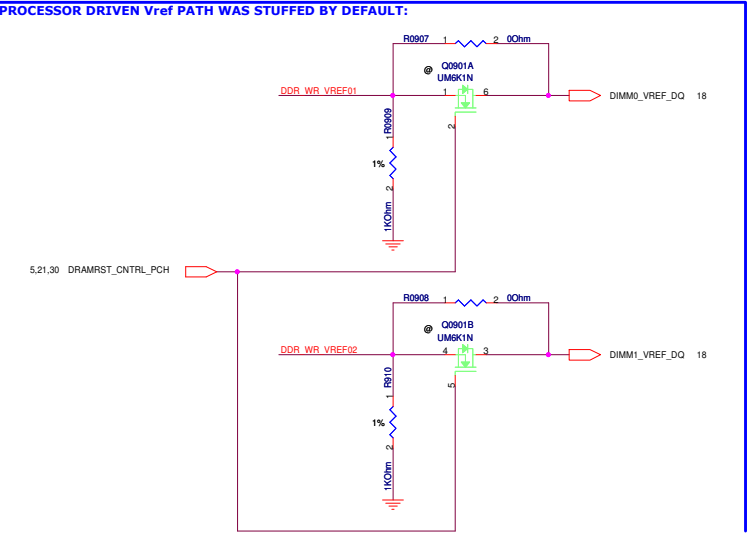
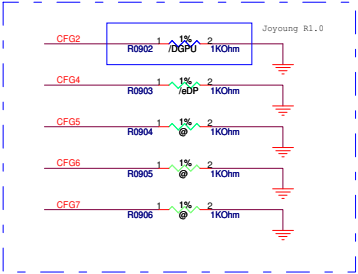


PEGATRON Title : CPU(5)_GFX_PWR

BG1-HW RD Div.2-NB RD Dept.5		Engineer:	Joyoung_Chianhg
Size C	Project Name JM50	Rev 3.1	
Date:	Thursday, August 23, 2012	Sheet	7 of 93



CFG strapping information:
CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x - 1: (Default) Normal Operation, Lane # definition matches socket pin map definition - 0: Lane Numbers Reversed
CFG[4]: Embedded DisplayPort Detection - 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort - 0: Enabled ; An external Display Port device is connected to the Embedded Display Port
CFG[6:5]: PCI Express Port Bifurcation Straps - 11 : (Default) x 1 6 - 10 : x 8 , x 8 - 01 : Reserved - 00 : x 8 , x 4 , x 4
CFG[7]: PEG DEFER TRAINING - 1: (Default) PEG Train immediately following xxRESETB de assertion - 0: PEG Wait for BIOS training



CPU XDP connector

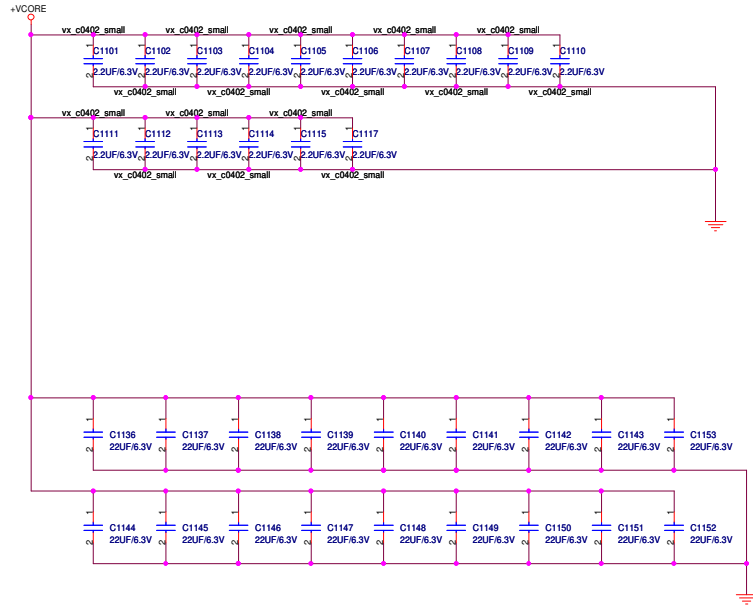
Check Connector

PCH XDP connector

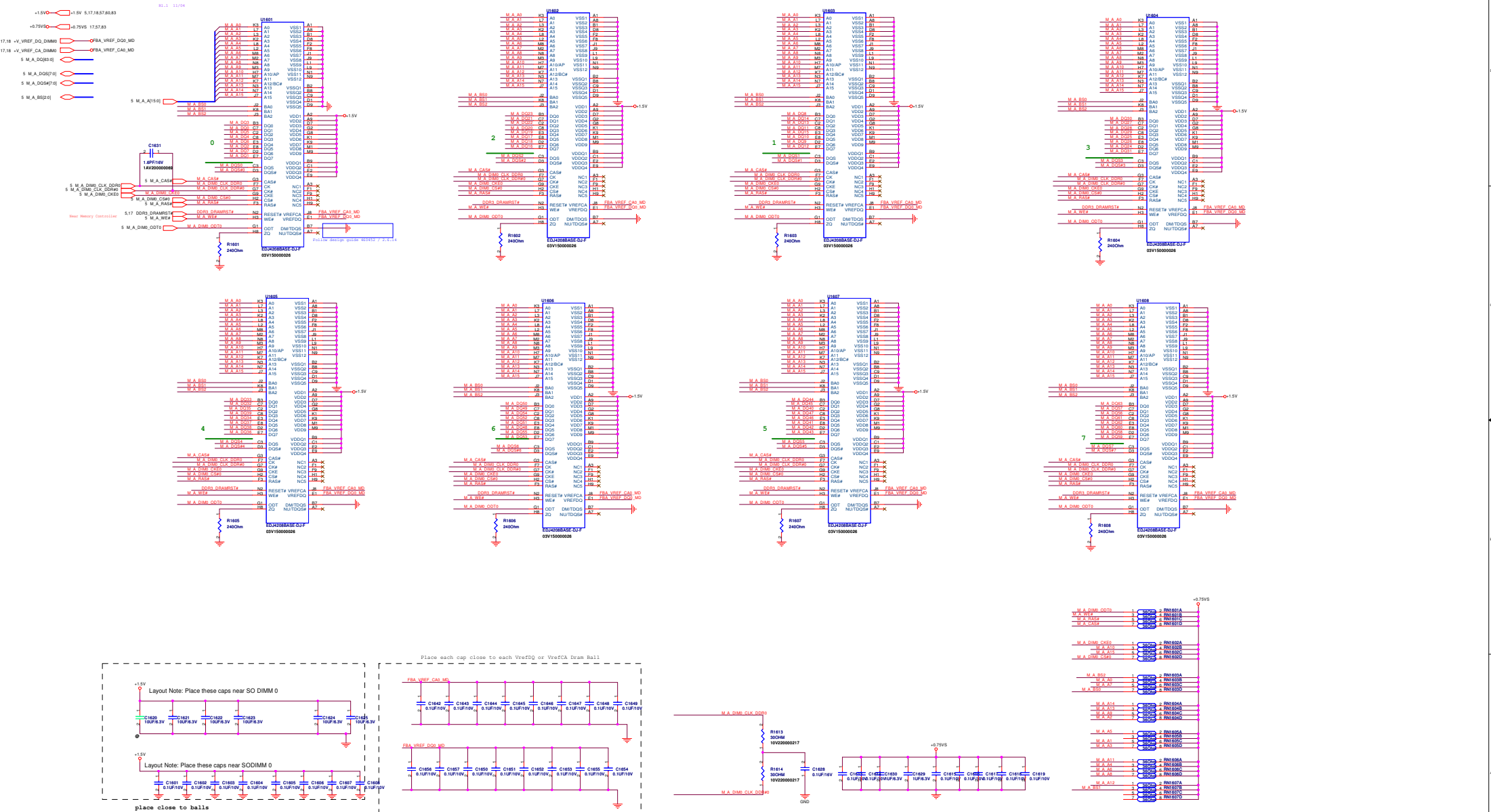
PEGATRON		Title : CPU_PCH_XDP	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	JM50		3.1
Date: Thursday, August 23, 2012		Sheet	10 of 93

Chief River
Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

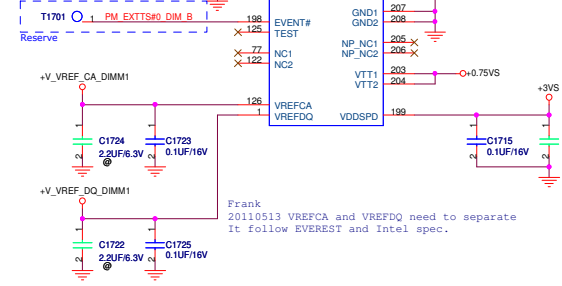
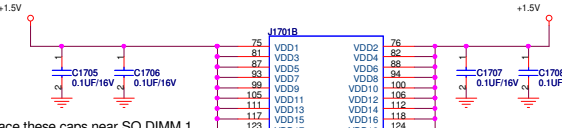
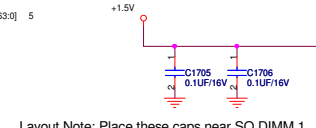
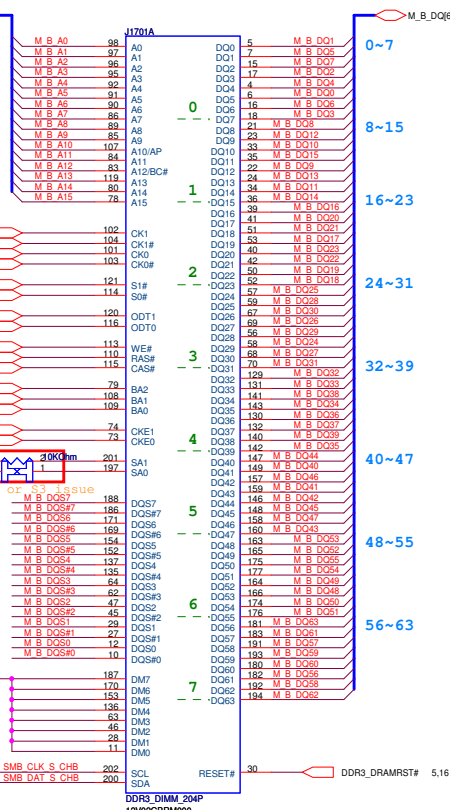
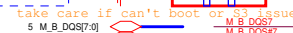
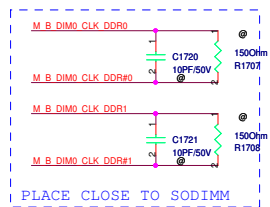
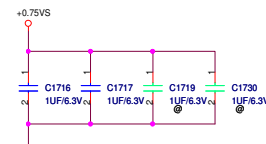
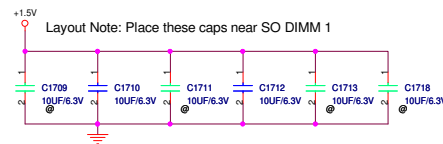
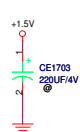
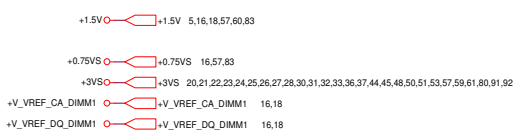
Chief River
+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



Memory Down CH A



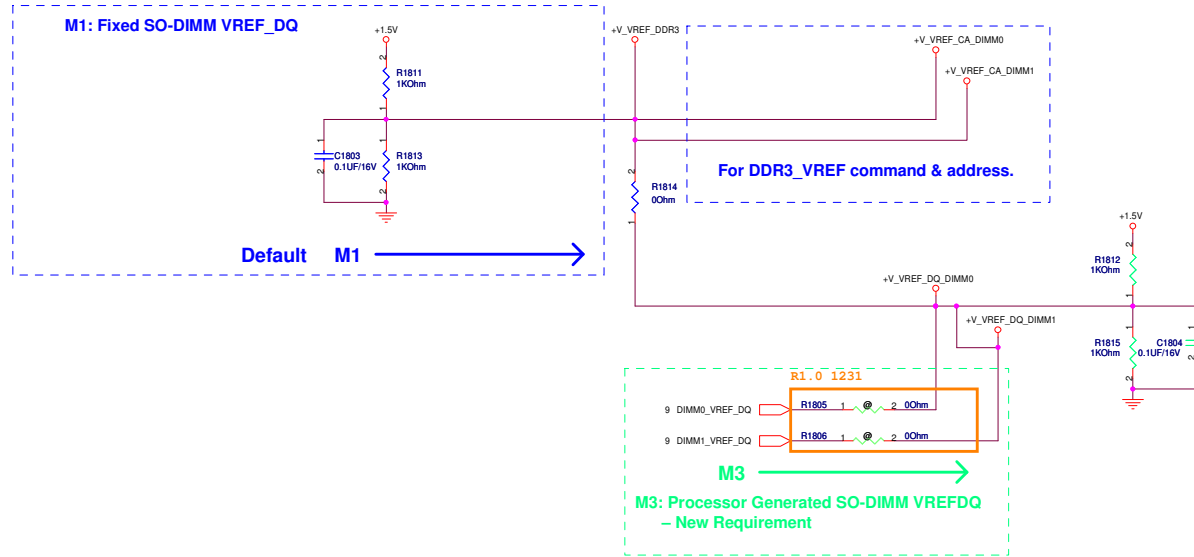
Title		Title	
801 488 RD Div 2 488 RD Dap1		Engineer: Jyoung Chnang	
Rev		Rev	
5		5	
Date		Date	
2017.10.10		2017.10.10	



Frank
20110513 VREFCA and VREFDQ need to separate
It follow EVEREST and intel spec.

H:5.2mm

DDR3 Vref



If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

+1.5V 5,16,17,57,60,83
 +V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 16,17
 +V_VREF_DQ_DIMM0 +V_VREF_DQ_DIMM0 16,17

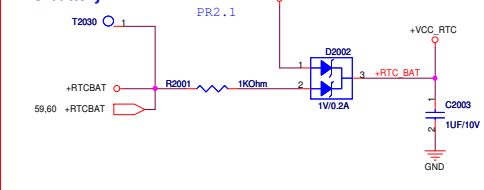
+3V 24,45,57,59,61,91
 +5VSUS 51,57,59,91
 +5VA 37,60,81,91

	5	4	3	2	1
D					
C					
B					
A					

R1.4--2

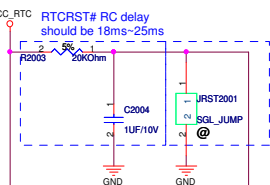
PEGATRON		Title : VID Controller	
PEGATRON COMPUTER INC		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	JMS0	3.1	
Date: Thursday, August 23, 2012		Sheet	19 of 83

RTC battery



Request by CSC
for CMOS clear
function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Intel I:5 Design Guide, page 260

isolate schematic for ACZ_SYNC and SDOUT follow EIH31

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

+VCC_RTC = +VCC_RTC 22,27

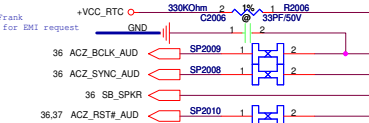
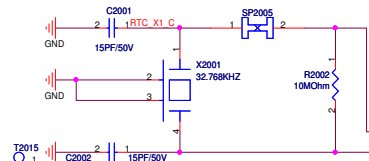
+3VA = +3VA 6,26,27,30,31,57,59,60,81,88,93

+3VS = +3VS 17,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

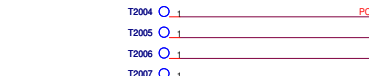
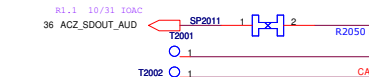
+3VSUS_ORG = +3VSUS_ORG 21,22,24,25,26,27,33

+VTT_PCH_VCCIO = +VTT_PCH_VCCIO 26,27

R1.0
Delete
+RTCBAT



Remove TP
ACZ_SYNC near R2008



COUGAR_POINT_ES1
02V000000001

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High: Enable

ACZ_SDOUT:

1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2. ACZ_SDOUT which sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector

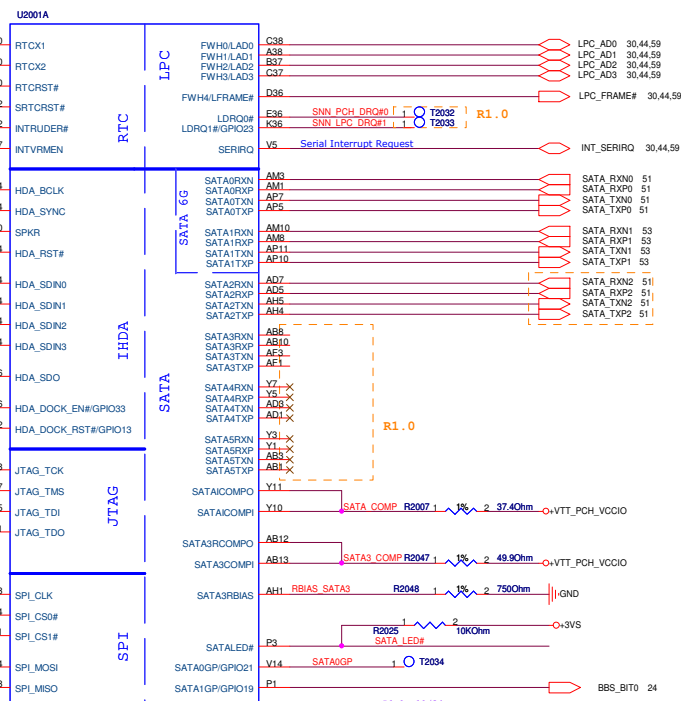
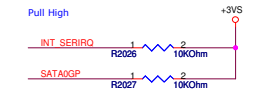
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hiron River Platform Schematic Design Checklist
(438390 page 48)

SB_SPKR = SB_SPKR 2 1KOhm +3VS

ACZ_SDOUT = ACZ_SDOUT 2 1KOhm +3VSUS_ORG

ACZ_SYNC = ACZ_SYNC 2 1KOhm +3VSUS_ORG

VCCVRAM use +1.5VS in mobile



PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC

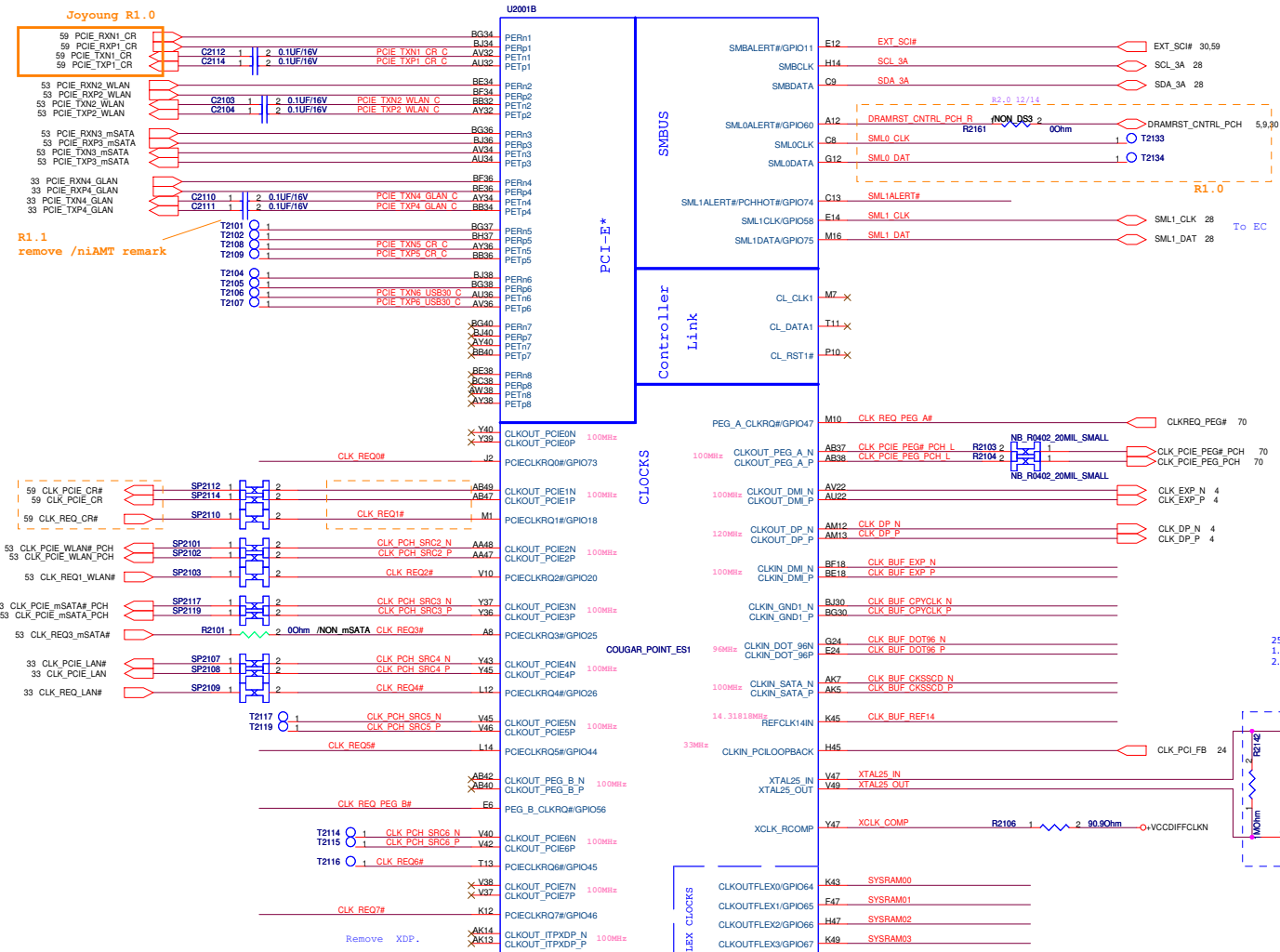
PEGATRON COMPUTER INC Engineer: Joyoung Chianhg

Size Project Name JM50 Rev 3.1

Date: Thursday, August 23, 2012 Sheet 20 of 93

Frank
0513_Add USB3.0 and Card Reader PCIE and CLKRQ

Frank
0517_Add 3G PCIE and CLKRQ in Port3.

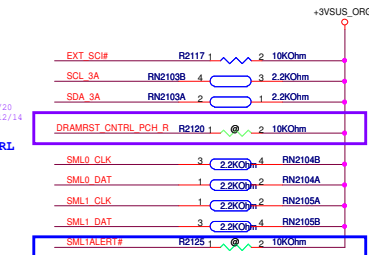
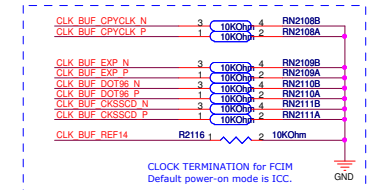


Joyoung R2.0
Add CLK10-5bit to fix on-board RAM Strap

On Board RAM Setting

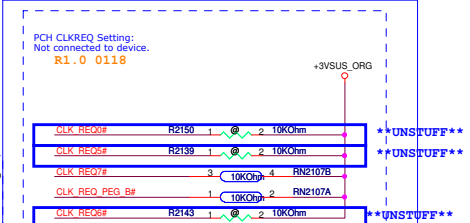
GPIO67	GPIO66	GPIO65	GPIO64	On Board RAM Setting
0000				No on board RAM
0001				Micron 1333MHz 4GB
0010				Elpida 1333MHz 4GB
0110				Elpida 1333MHz 2GB
0101				Micron 1333MHz 2GB
0100				Hynix 1333MHz 2GB
XXXX				TBD
1000				Common Definition 1333MHz 4GB
1001				Common Definition 1600MHz 4GB
0111				Elpida 1600MHz 2GB

+3VS 17,20,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+VTT_PCH_ORG 22,26,27
+3VSUS_ORG 20,22,24,25,26,27,33

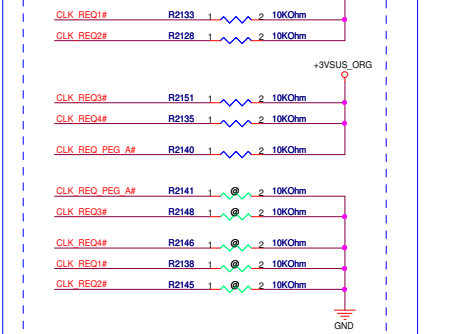


Joyoung R1.0 modify CLK_REQ

- 25-MHz is required in:
 - 1. FCIM
 - 2. BTM for PCH Display Clock generation in Integrated Graphics platforms



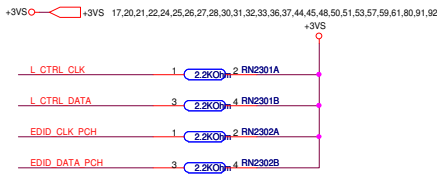
Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
Eric Fang to Alan Chien on 11/15/2010



PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG

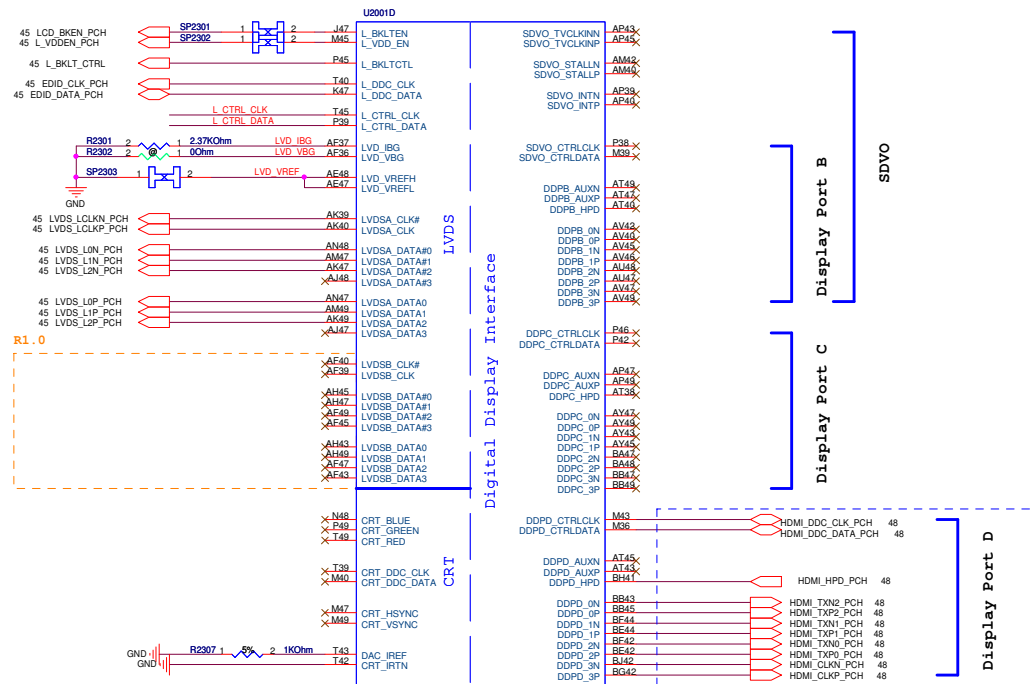
PEGATRON COMPUTER INC Engineer: Joyoung Chianhg

Size Project Name JM50 Rev 3.1
Date: Thursday, August 23, 2012 Sheet 21 of 93



Pull up 2.2k ohm in DDC bus for LVDS .

Remove LVDS net name and add port B.



COUGAR_POINT_ES1
02V000000001

CRT Disable: (For discrete graphic)

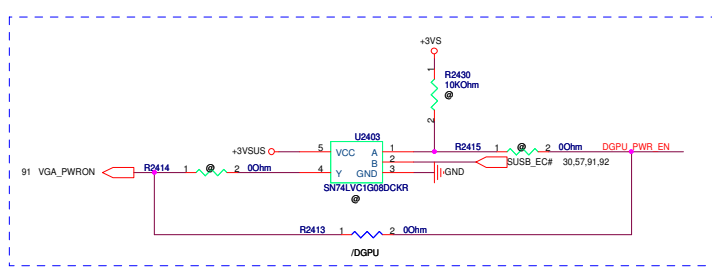
1. NC:
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYNC,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:
ALL

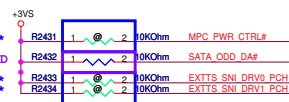
LVDS Disable: (For discrete graphic)

1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS,VccTX_LVDS



Frank
20110608 SP2401 is removed in E1H31.
SATA_ODD_DA# has short pin in E1H31.

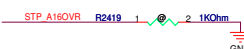
****UNSTUFF****
R1.1 add Zero Power ODD
****UNSTUFF****
R2431 1K0Kohm MPC_PWR_CTRL#
R2432 1K0Kohm SATA_ODD_DA#
R2433 1K0Kohm EXITS_SNI_DRV0_PCH
R2434 1K0Kohm EXITS_SNI_DRV1_PCH



STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

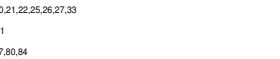
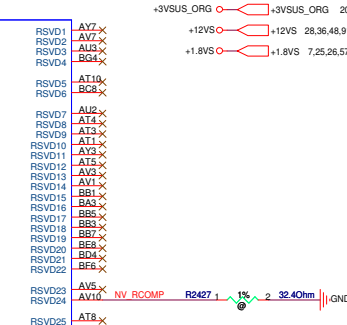
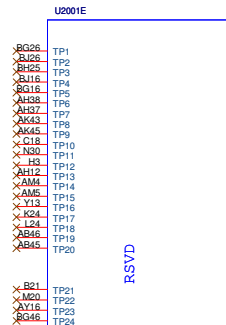
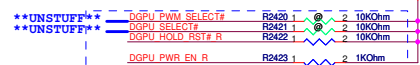
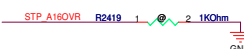
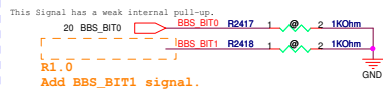
High=Default



BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

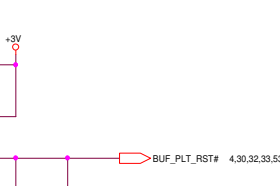
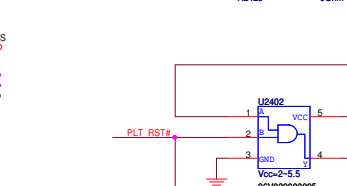
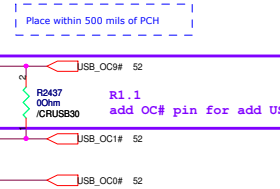
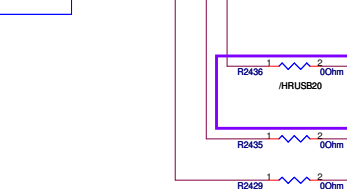
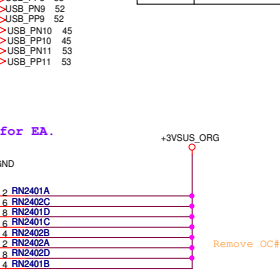
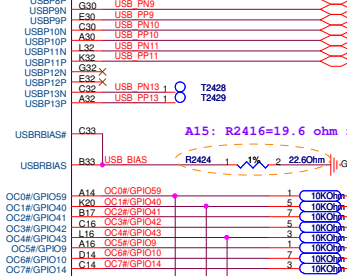
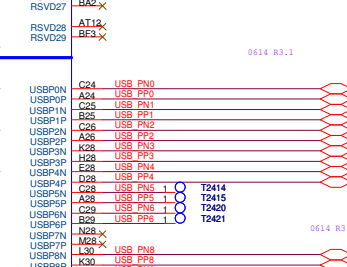
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI (PCH)

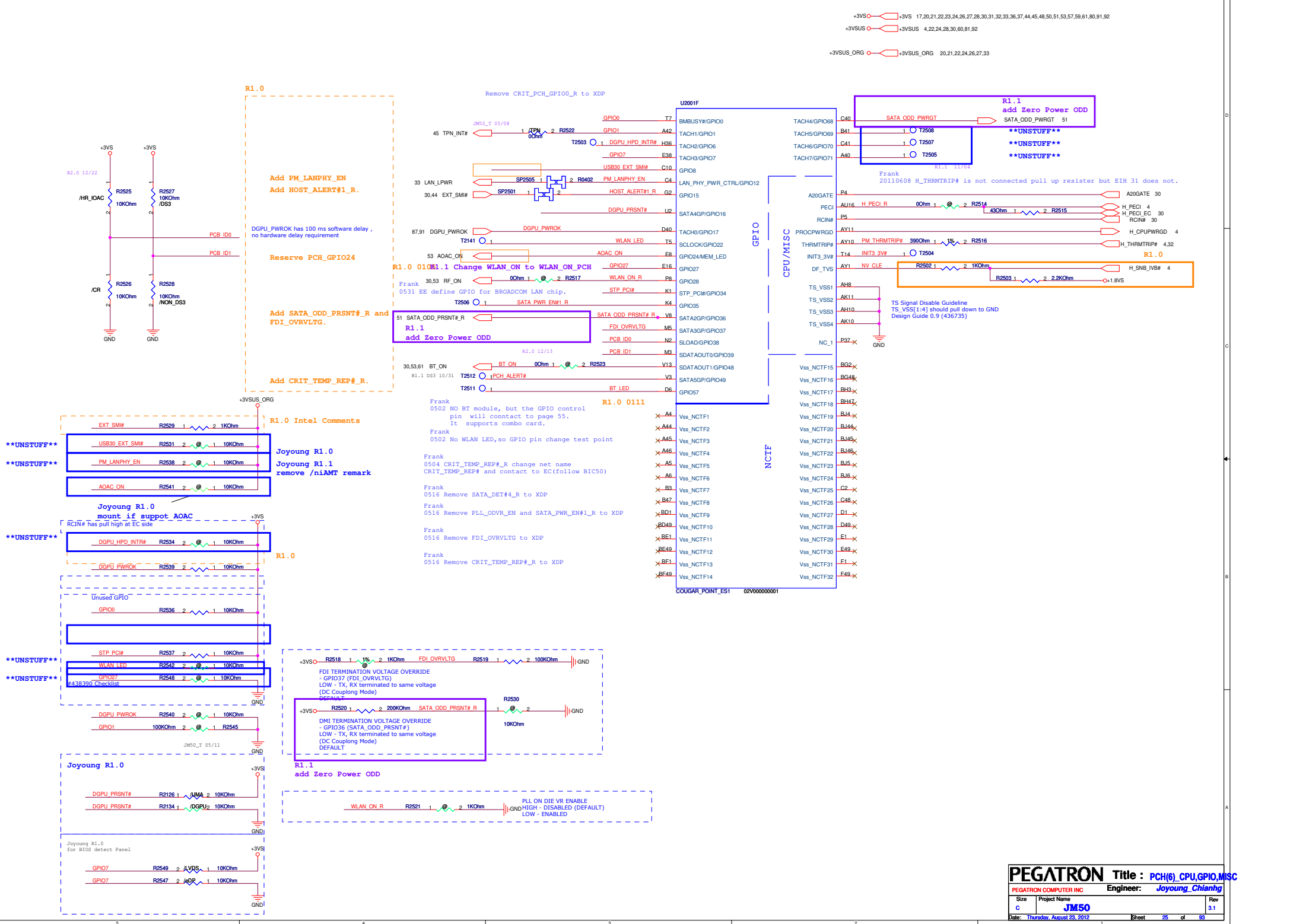
Sampled on rising edge of PWROK.

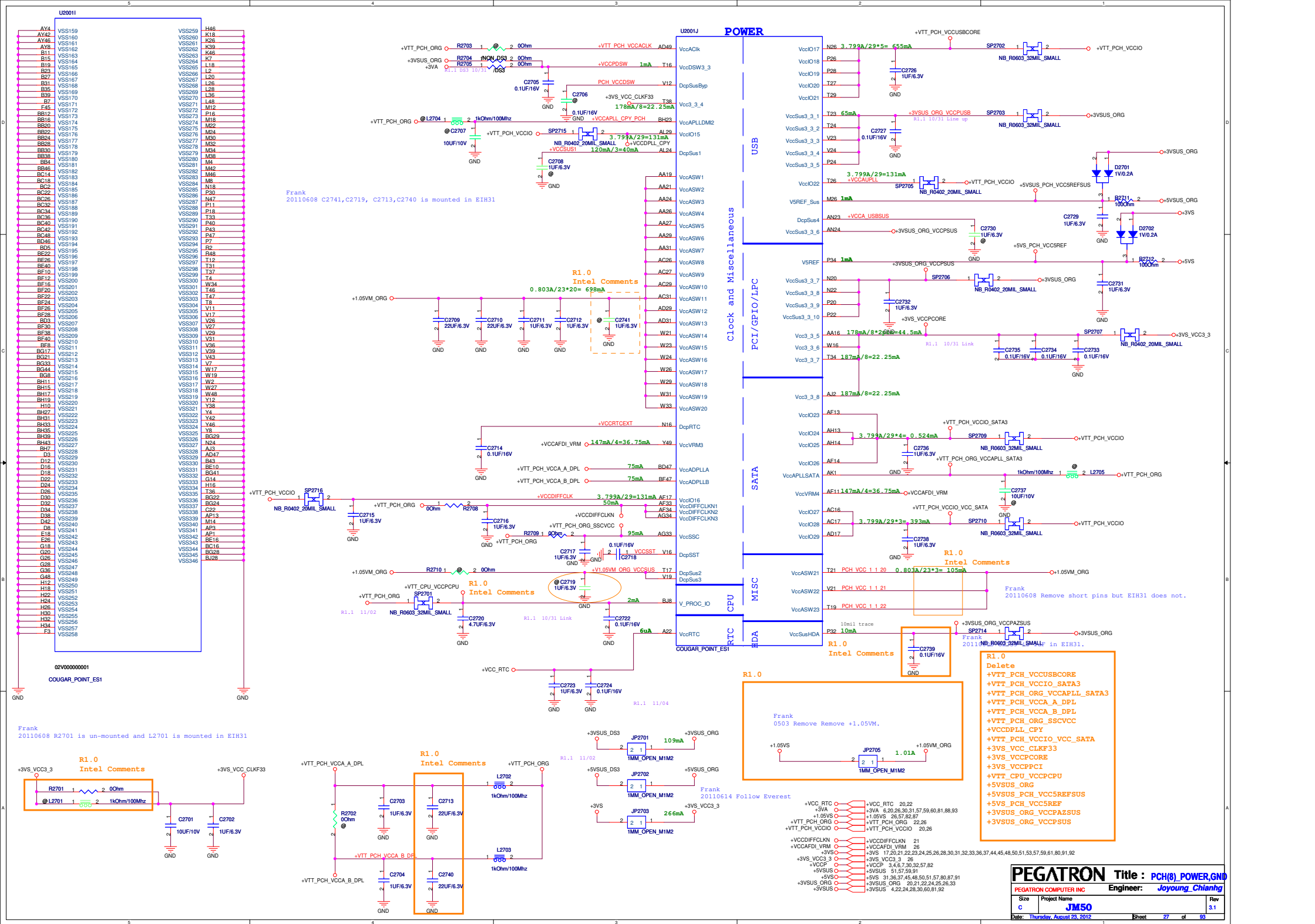


USB PORT

USB P00	Touch Panel
USB P01	External 2.0/3.0
USB P02	External Main
USB P03	External Main
USB P04	BT
USB P05	
USB P08	Mini PCIE (mSATA)
USB P09	Debug Port
USB P10	Camera
USB P11	WiFi
USB P12	
USB P13	







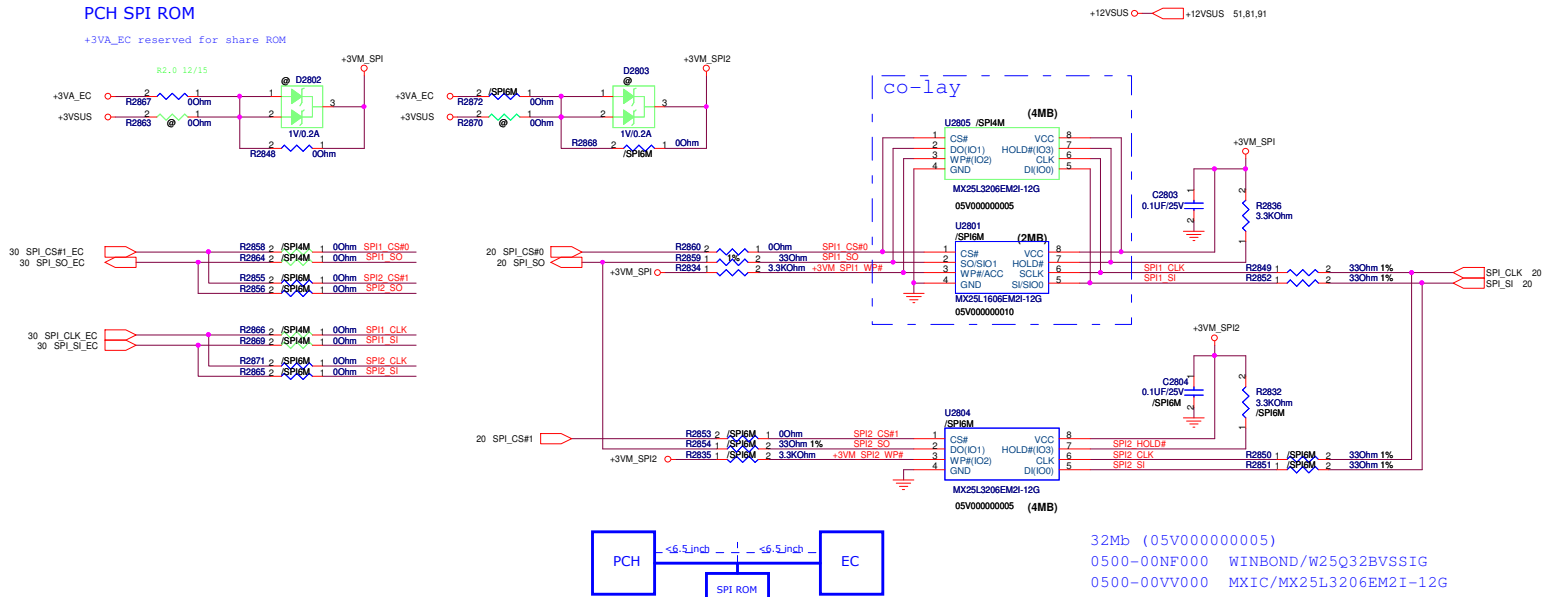
PCH SPI ROM

SHARE ROM CONFIG1

U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB
ummount: R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802, R2869, R2870, R2868, D2802, U2801		

SHARE ROM CONFIG2

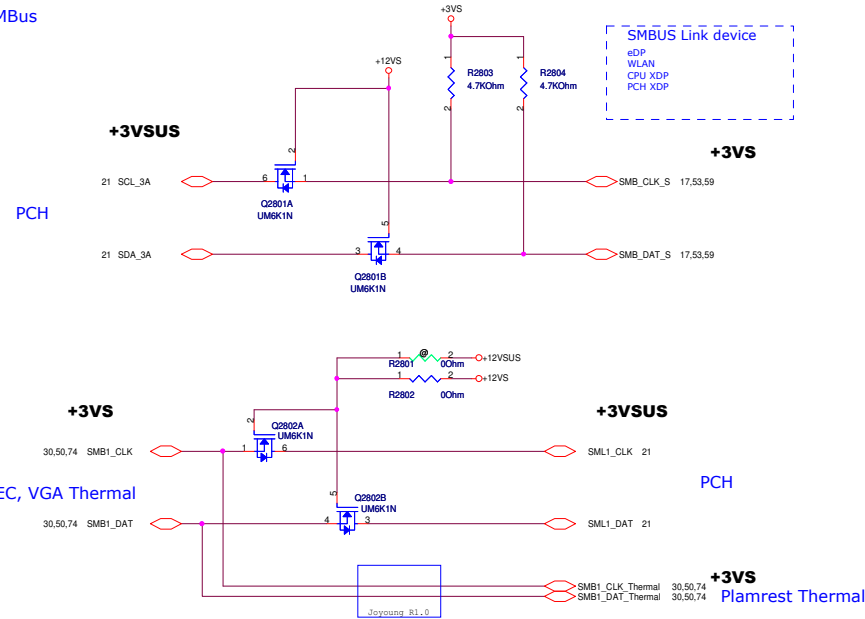
U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB
ummount: R2858, R2862, R2866, R2867, U2803		



SPI Debug Connector

layout space issue, so remove J2801.

PCH SMBus

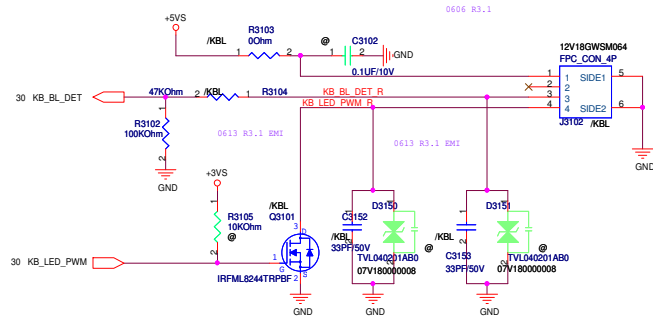


	5	4	3	2	1
D					
C					
B					
A					

PEGATRON		Title : CLK_JCS9LRS3197	
PEGATRON COMPUTER INC		Engineer: Joyoung_Chianhg	
Size Custom	Project Name JM50		Rev 3.1
Date: Thursday, August 23, 2012		Sheet 29	of 93

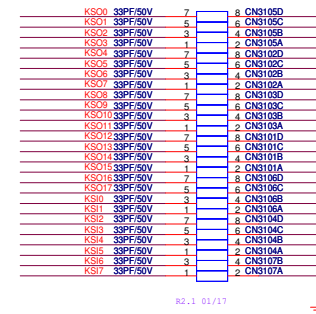
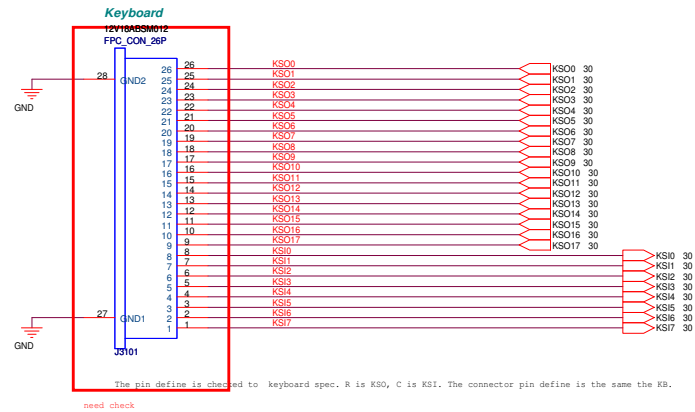
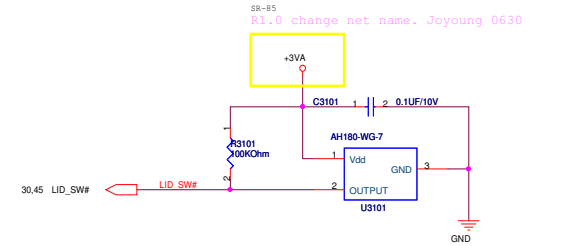
KB backlight




R3.1 Add 4P CON for KB Backlight Kevin 0601



LID Switch

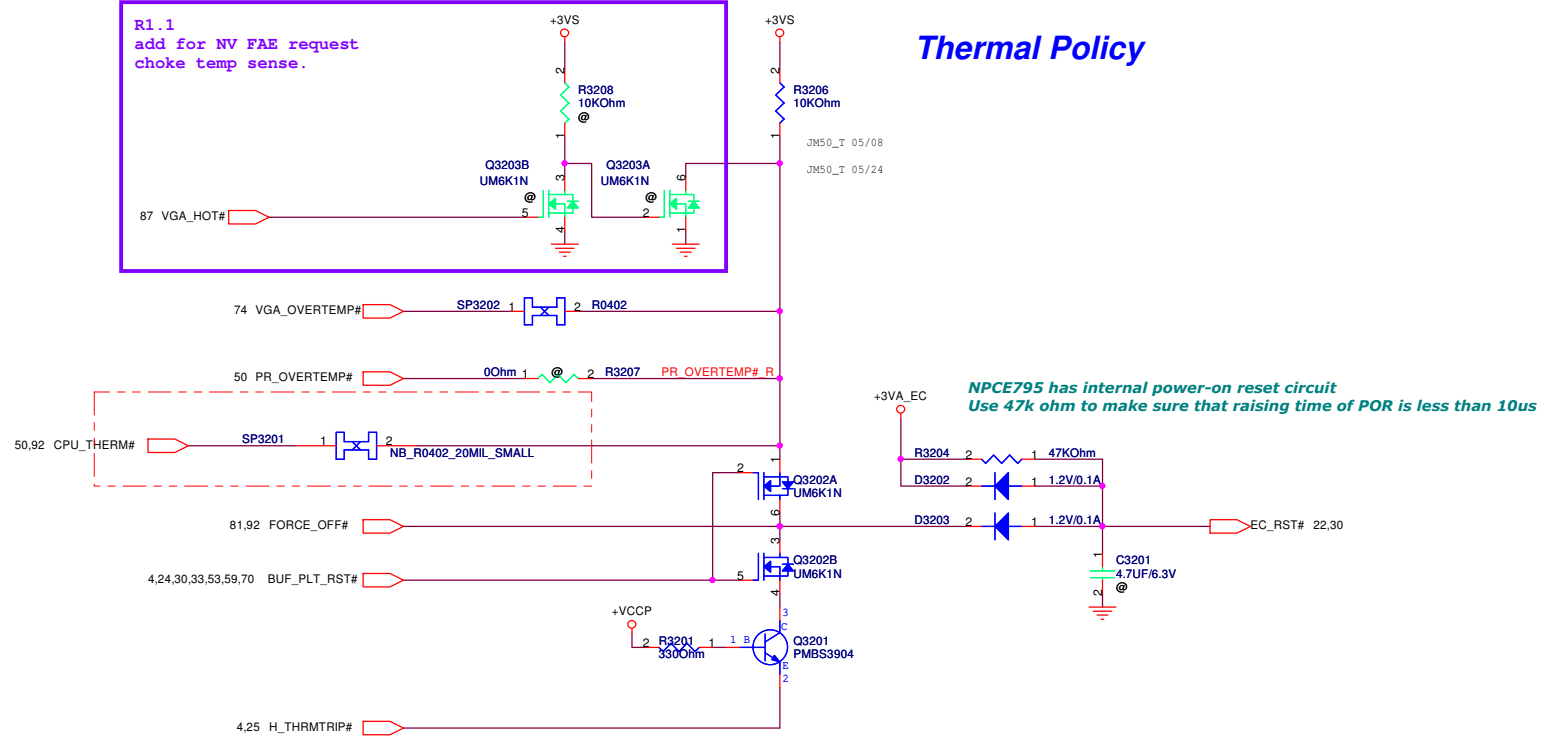
R1.0 change net name. Joyoung 0630

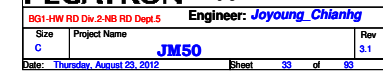


+VCCP  +VCCP 3,4,6,7,30,57,82
 +3VA_EC  +3VA_EC 28,30
 +3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,31,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

R1.1
 add for NV FAE request
 choke temp sense.

Thermal Policy





Joyoung R1.0
FAE suggest common mode choke is on chip side.

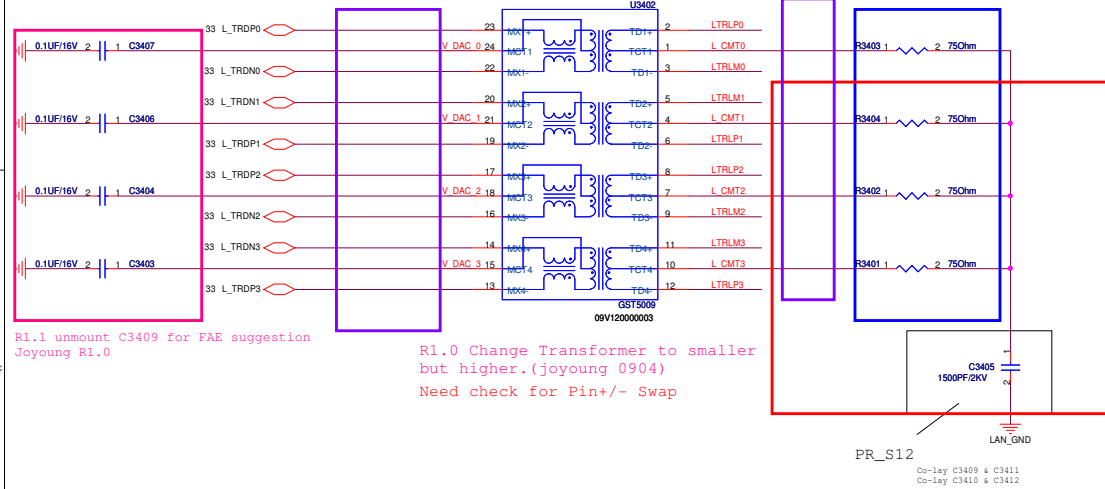
R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405-R3407 & C3409

R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

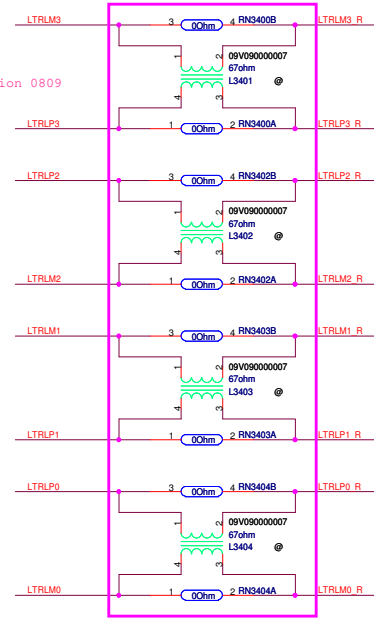
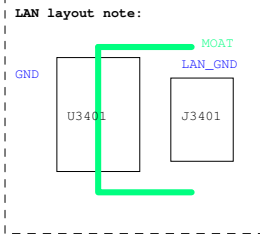
R1.1 Mount R3401-R3403 for FAE suggestion 0809



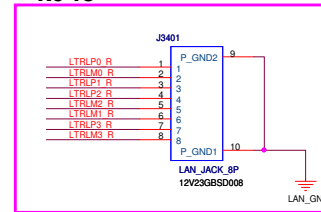
R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

R1.0 Change Transformer to smaller
but higher. (joyoung 0904)
Need check for Pin+/- Swap

PR_S12
Co-lay C3409 & C3411
Co-lay C3410 & C3412



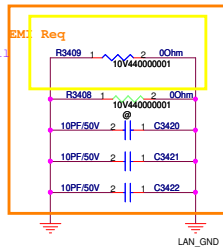
RJ45



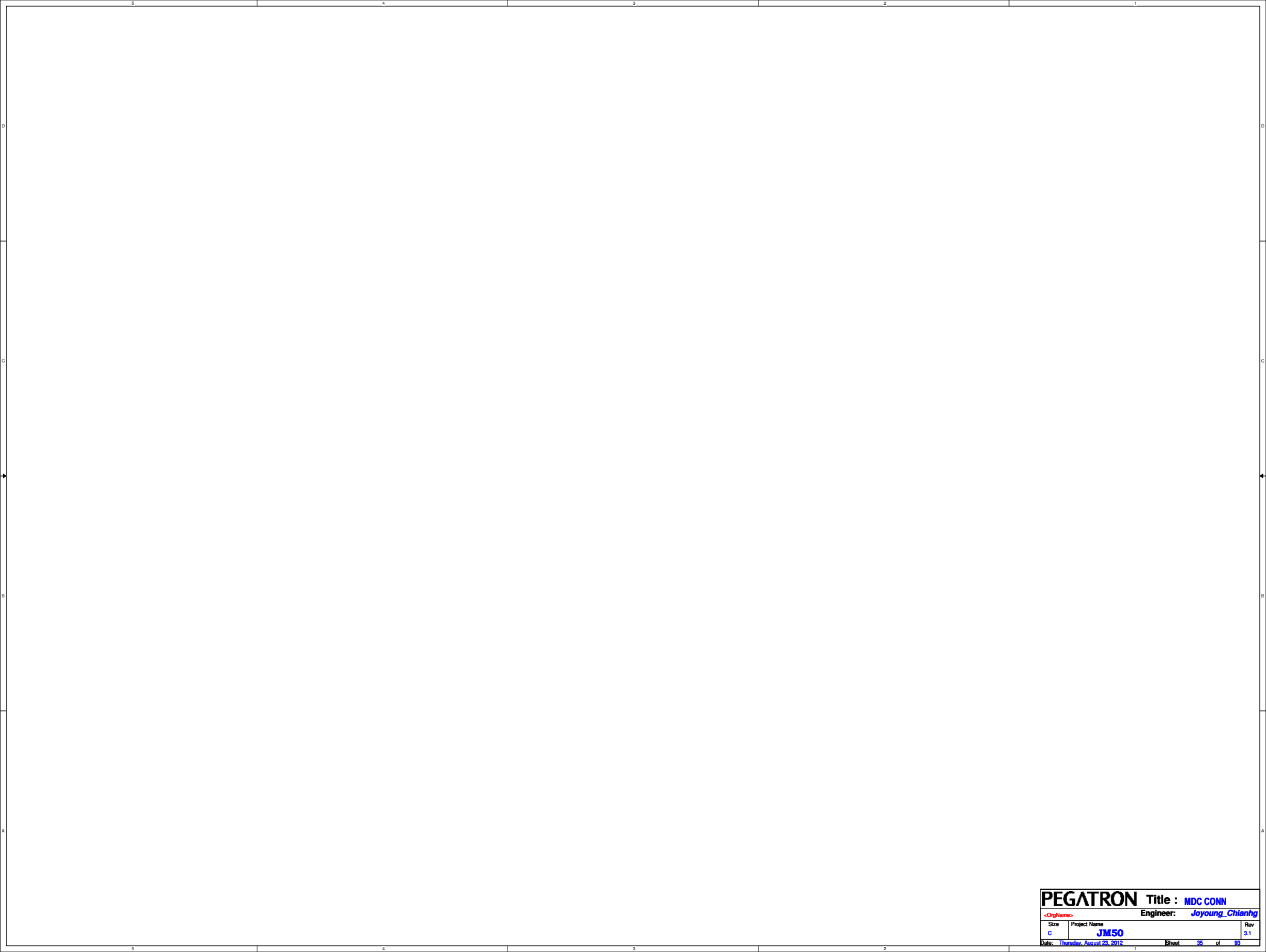
Change RJ45 CON3401

R1.0 Reserve D3401 for EMI.

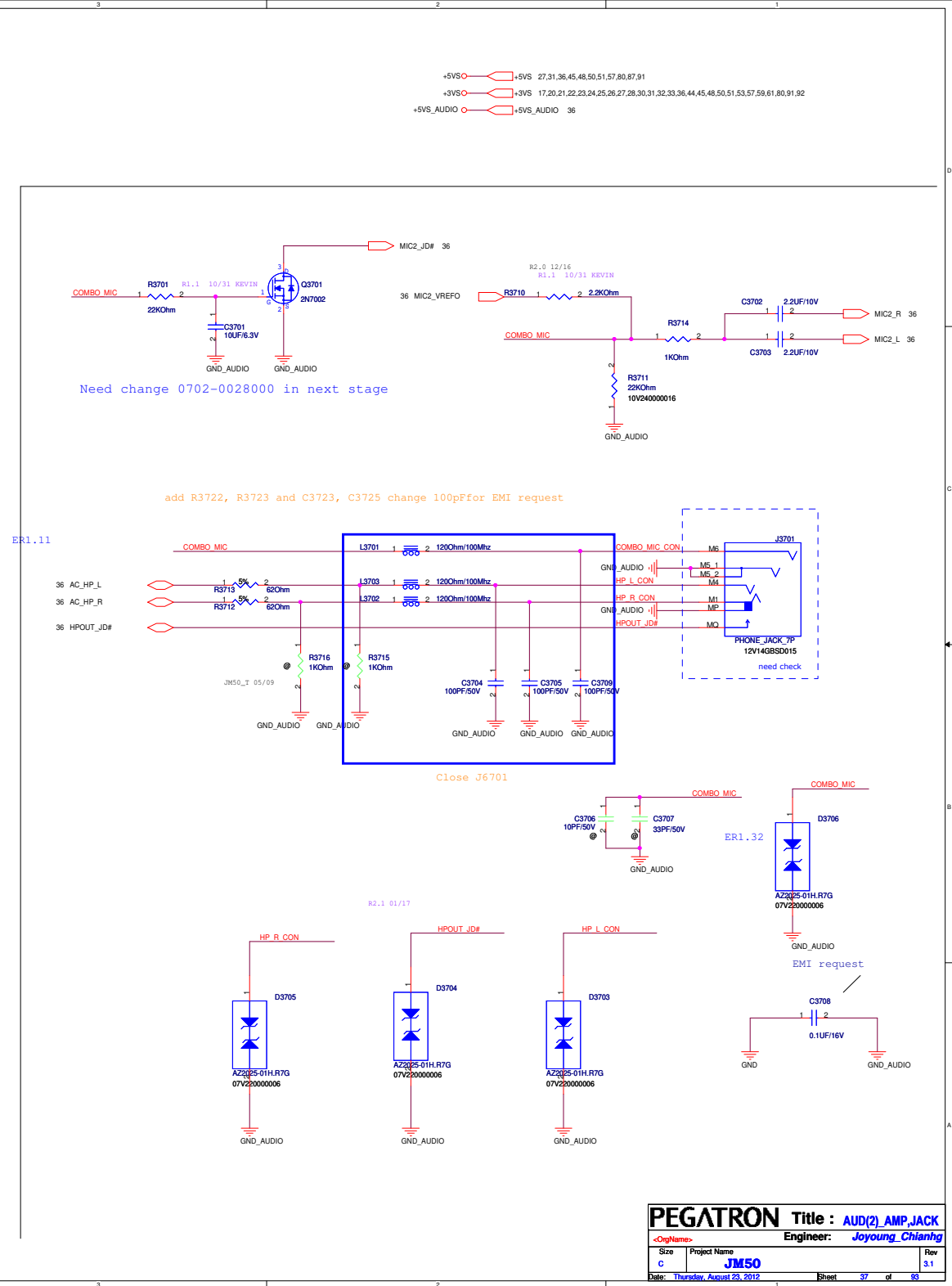
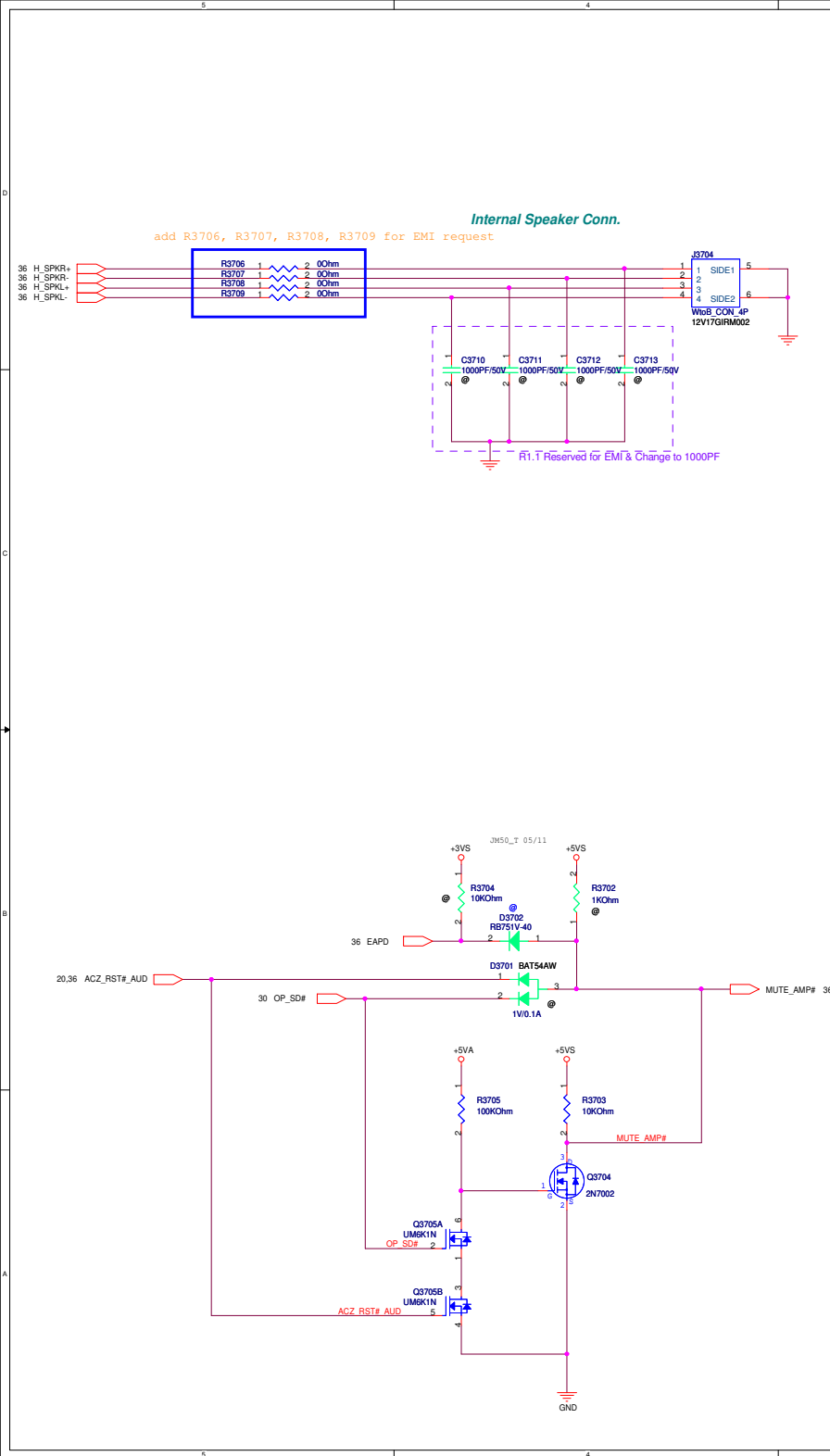
R1.0 Mount R3408 for FAE suggestion



R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all

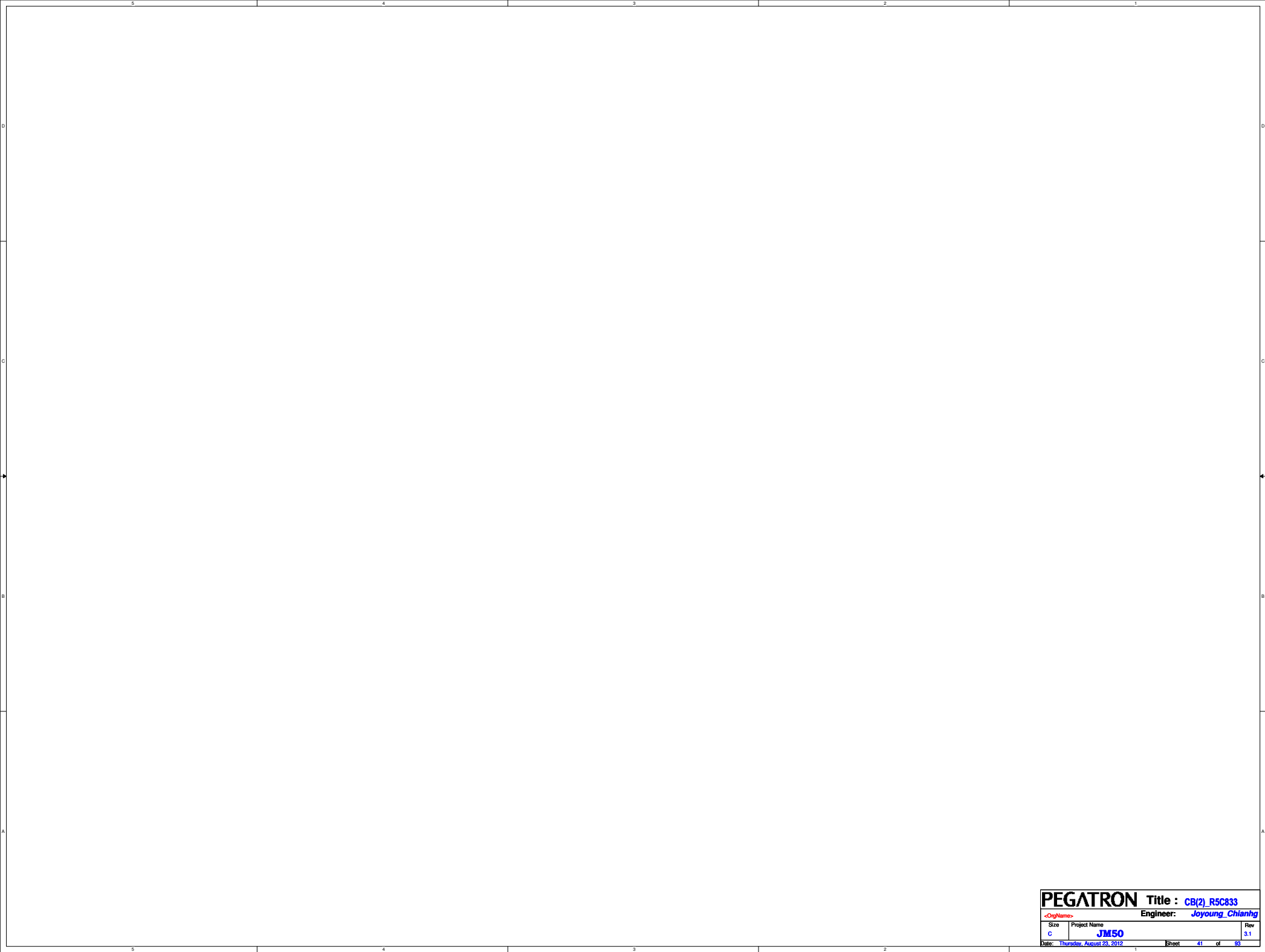




PEGATRON		Title : MDC CONN	
<OrigName>		Engineer: Joyoung Chianhg	
Size	Project Name		Rev
C	JM50		3.1
Date: Thursday, August 23, 2012		Sheet	35 of 83





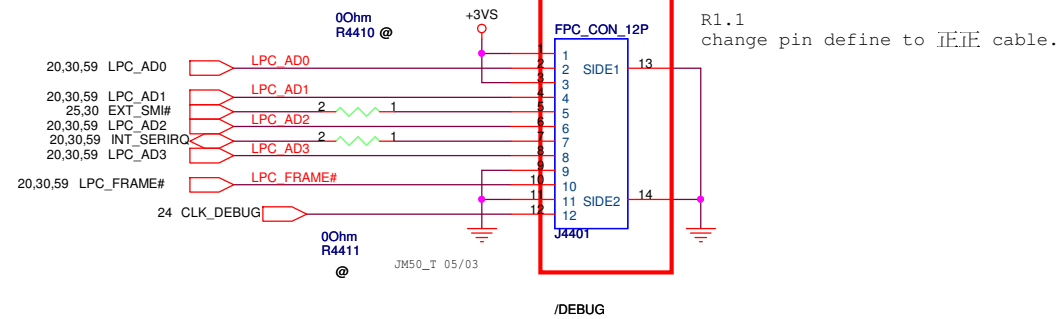
PEGATRON		Title : AUD(4) ****	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	JM50		3.1
Date: Thursday, August 23, 2012		Sheet	39 of 93



+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+12V  +12V 60,91

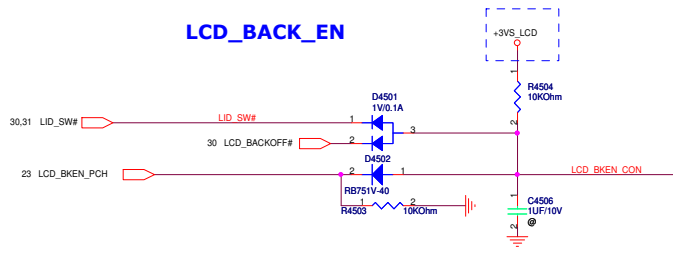
+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

LPC Debug Port

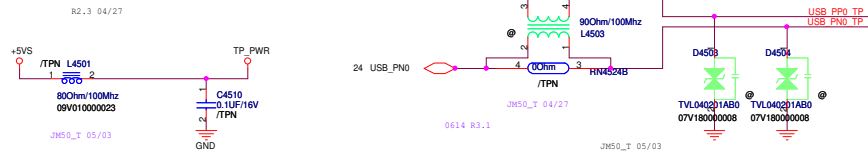


PEGATRON		Title : BUG_Debug	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
B	JM50		3.1
Date: Thursday, August 23, 2012		Sheet	44 of 93

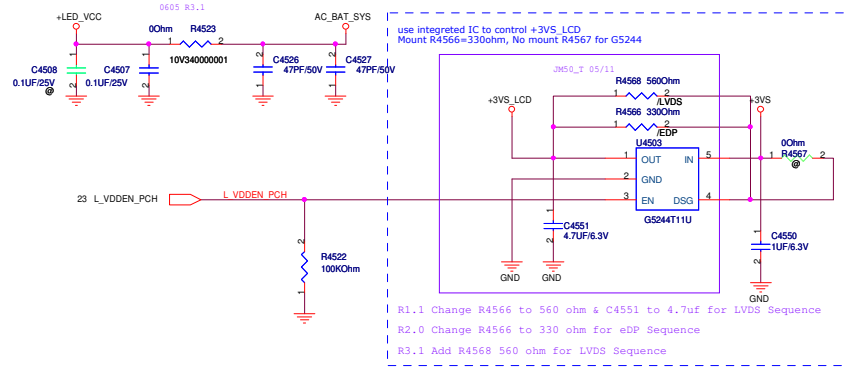
LCD_BACK_EN



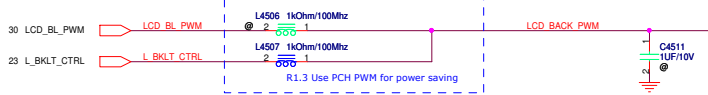
Touch Panel



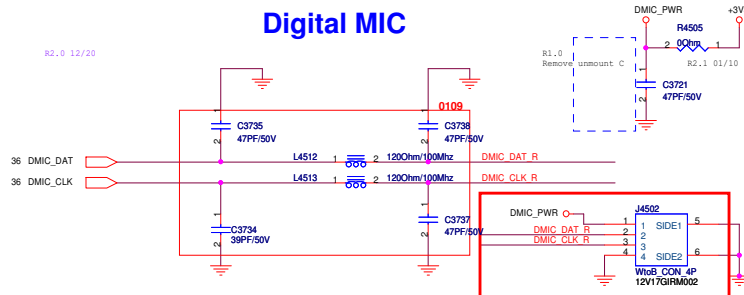
LCD VDDEN / +LED_VCC



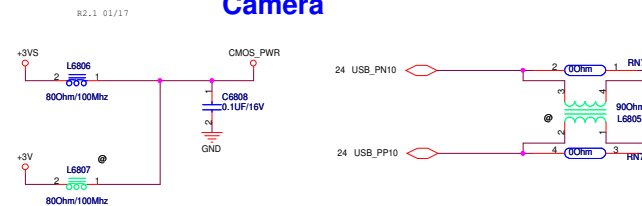
LCD_BL_PWM



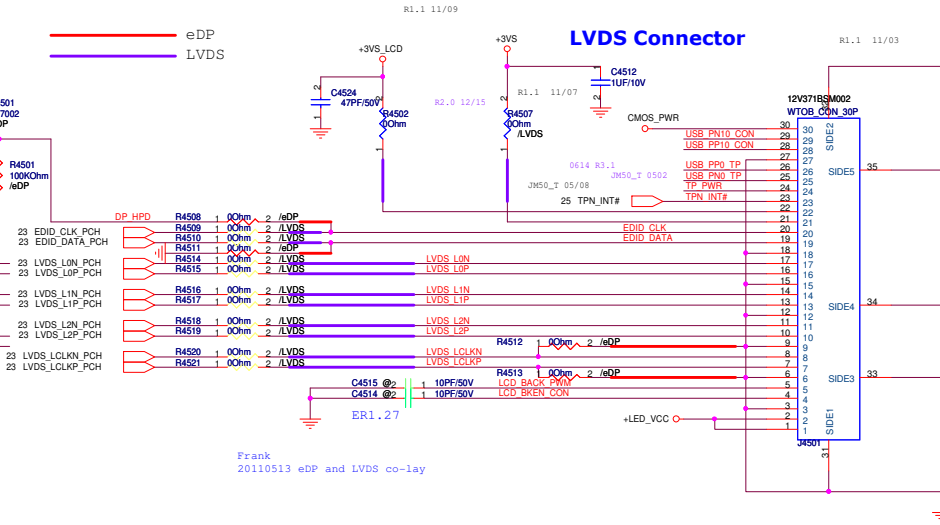
Digital MIC



Camera

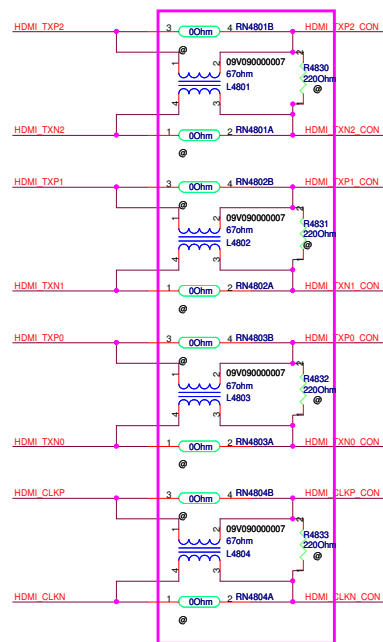
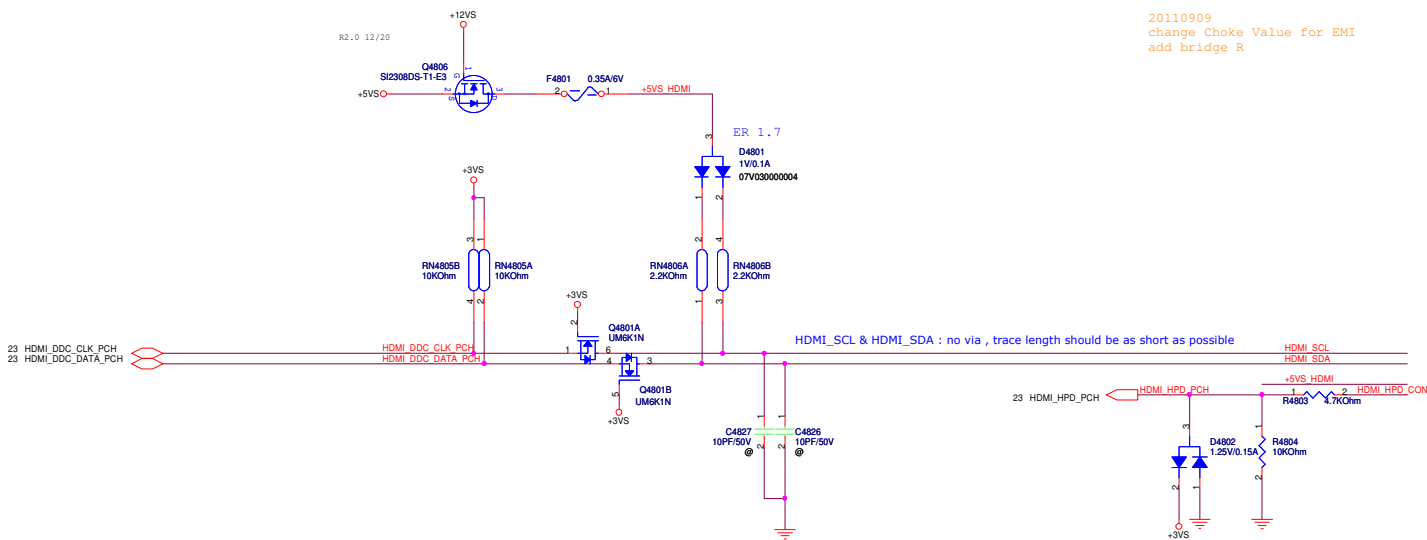
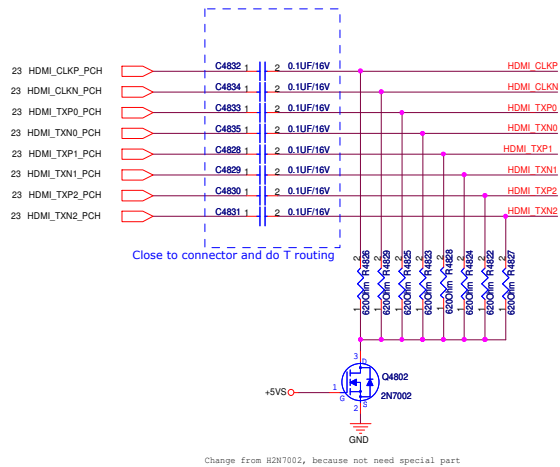


LVDS Connector

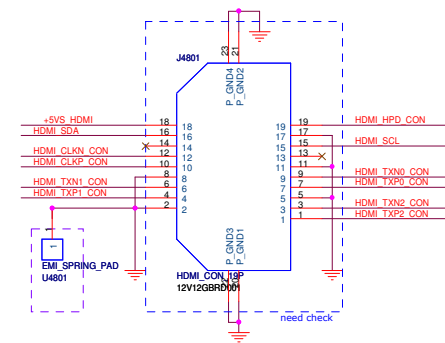




PEGATRON		Title : CRT	
BU1-RD Div.1-HW RD Dept.1		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	JM50		3.1
Date: Thursday, August 23, 2012		Sheet 46 of 93	



20110909
change Choke Value for EMI
add bridge R

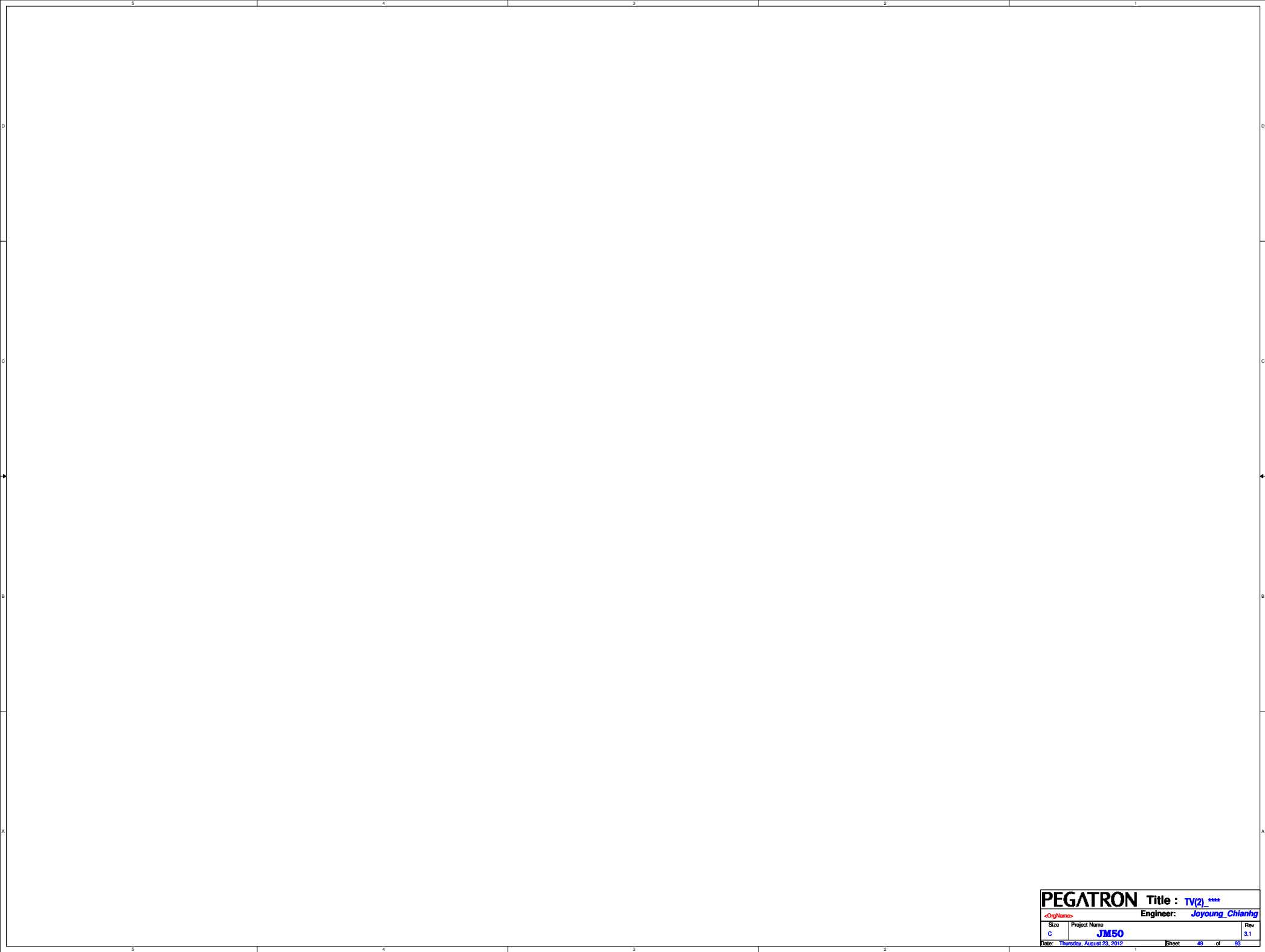


R1.1 EMI Request for Spring PAD(close to HDMI conn)

+12VS 28.36,91

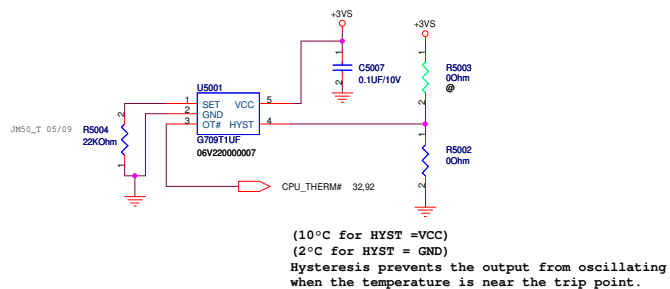
+3VS 17.20,21.22,23.24,25,26,27,28,30,31,32,33,36,37,44,45,50,51,53,57,59,61,80,91,92

+5VS 27.31,36,37,45,50,51,57,80,87,91



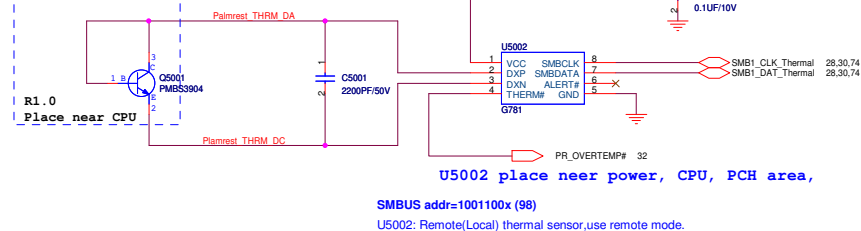
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,51,53,57,59,61,80,91,92
+5VS 27,31,36,37,45,48,51,57,80,87,91

CPU Thermal Sensor

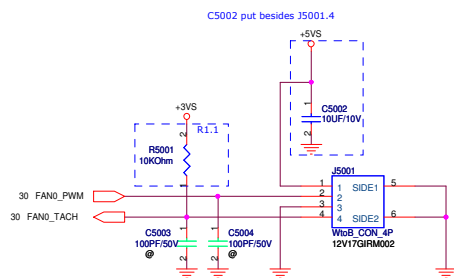


DIMM Thermal Sensor

PHILIP PMBS3904
Please in the center of Plamrest.

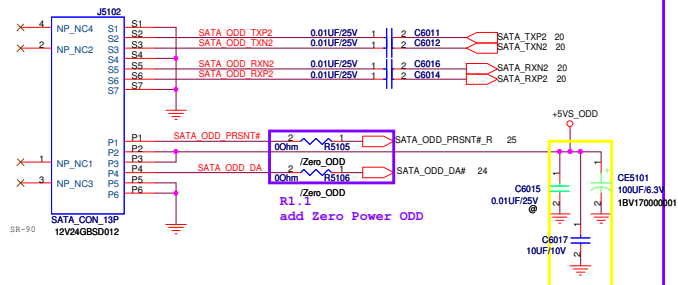


PWM Fan



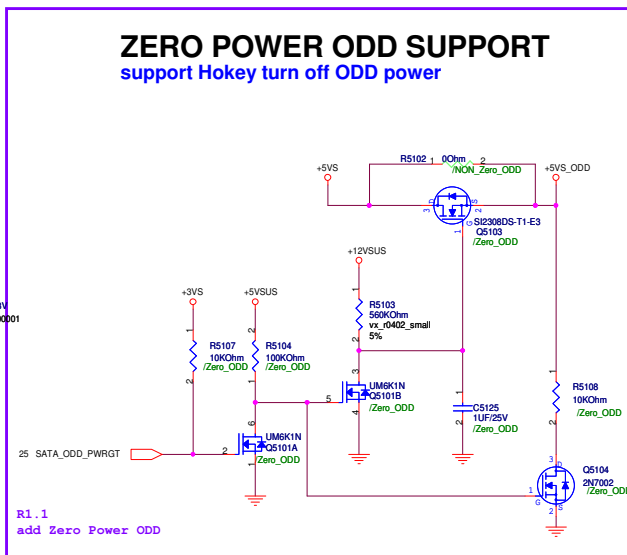
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,53,57,59,61,80,91,92
+5VS 27,31,36,37,45,48,50,57,80,87,91

ODD

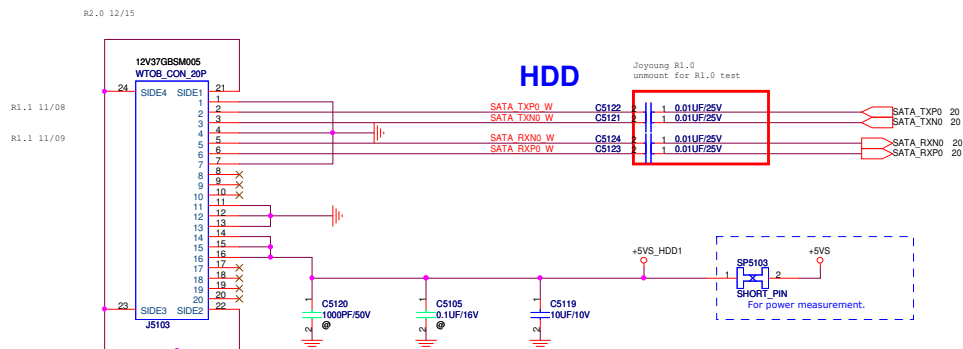


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



Connector for Cable



CH1(MB) : pin 8, 9, 10, 17, 18, 19, 20, NC 不接線
CH2(HDD) : P1, P2, P3, P10, P11, P12, P13, P14, P15, NC 不接線

R1.1 11/02 Remove HDD SATA CONN PART

PEGATRON		Title : <u>USB3.0</u>	
<OrgName>		Engineer: <u>Joyoung_Chianhg</u>	
Size B	Project Name JM50	Rev 3.1	
Date: <u>Thursday, August 23, 2012</u>		Sheet <u>54</u>	of <u>93</u>



+3VA 6,20,26,27,30,31,57,59,60,81,88,93
+3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,46,50,51,53,57,59,61,80,91,92
+SVSUS 51,57,59,91
+5VA 37,60,81,91
+5V 57,59,60,91
+SVS 27,31,36,37,45,46,50,51,57,80,87,91
AC_BAT_SYS 45,53,81,87,88
+3V 24,45,57,59,61,91

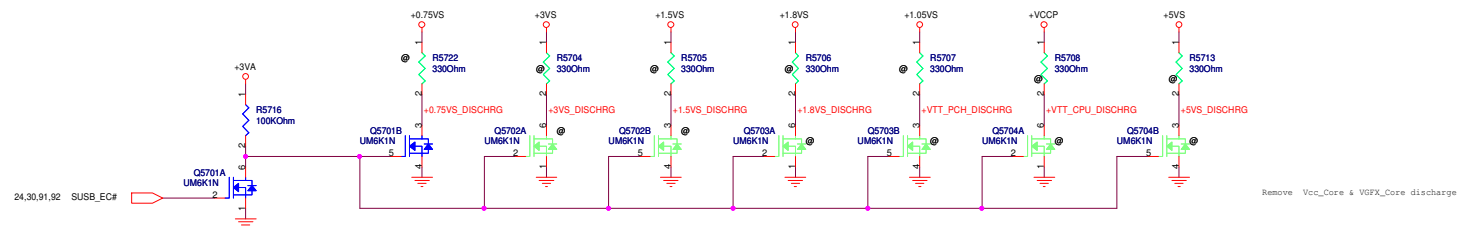
30.59 PWR_LED#

30.59 PWR_LED_standby#

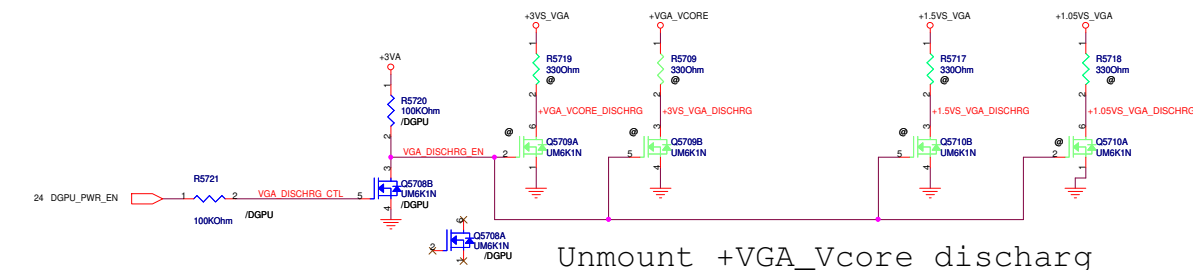
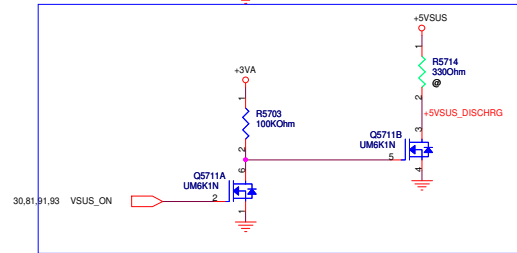
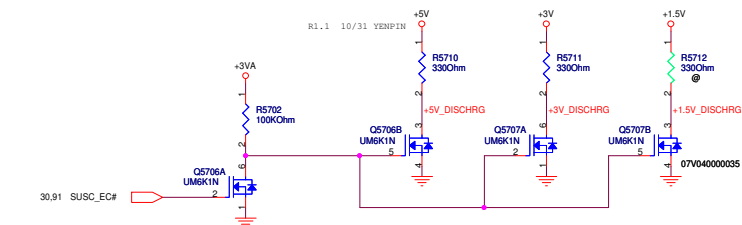
30.59 CHG_LED_BLUE#

30.59 CHG_LED_ORANGE#

- +3VA ○ 3VA 6,20,26,27,30,31,59,60,81,88,93
- +VOCORE ○ VOCORE 6,8,11,80
- +VGFX_CORE ○ VGFX_CORE 7,9,80
- +VCCP ○ VCCP 3,4,6,7,30,32,82
- +0.75VS ○ 0.75VS 16,17,83
- +1.05VS ○ 1.05VS 26,27,82,87
- +1.5VS ○ 1.5VS 7,26,53,91
- +1.8VS ○ 1.8VS 7,25,26,80,84
- +3VS ○ 3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92
- +5VS ○ 5VS 27,31,36,37,45,48,50,51,80,87,91
- +1.5V ○ 1.5V 5,16,17,18,60,83
- +3V ○ 3V 24,45,59,61,91
- +5V ○ 5V 59,60,91



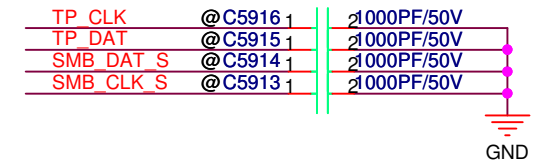
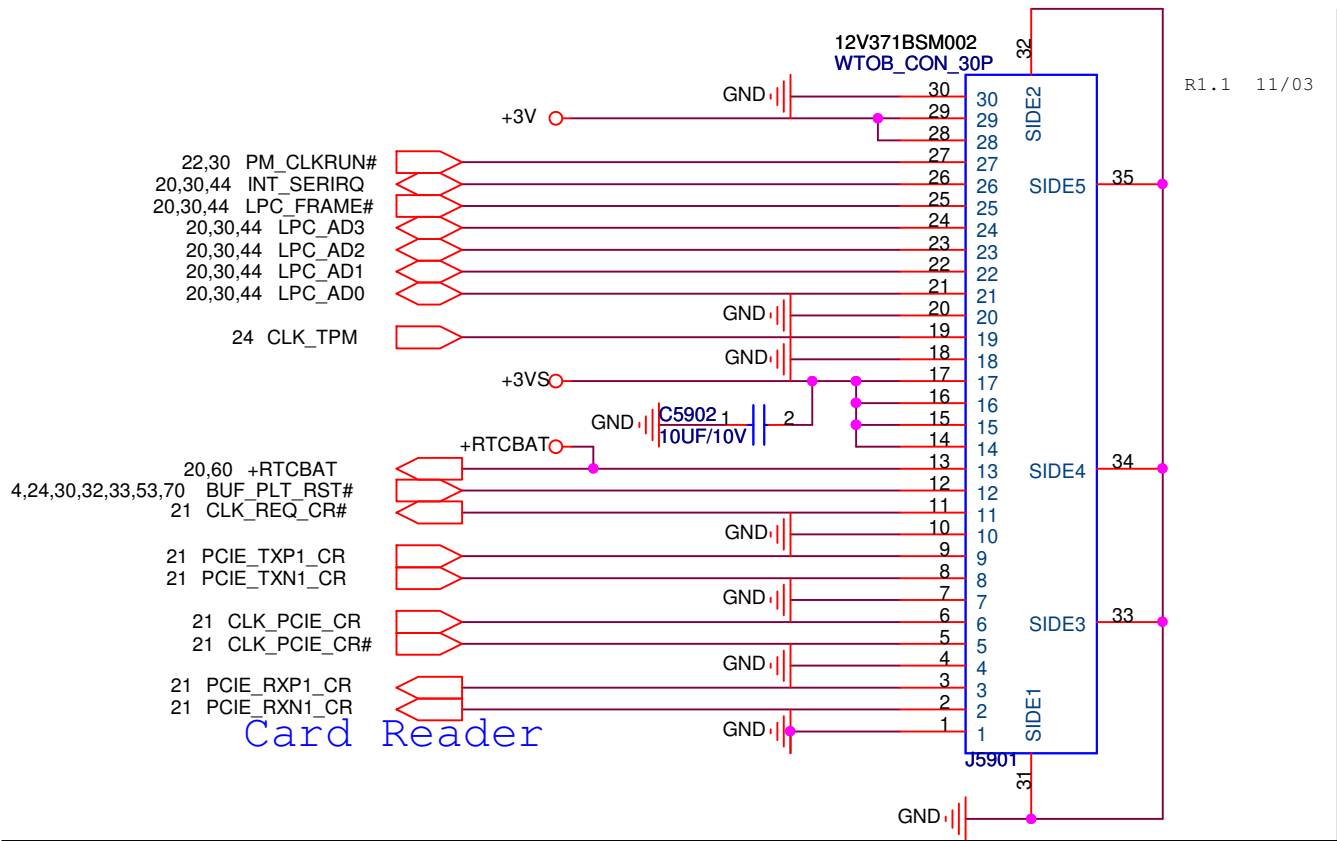
Remove Vcc_Core & VGFX_Core discharge



Unmount +VGA_Vcore discharg

PEGATRON		Title : <u>DSG_Discharge</u>	
<OrgName>		Engineer: <u>Joyoung_Chianhg</u>	
Size	Project Name		Rev
<u>C</u>	<u>JM50</u>		<u>3.1</u>
Date: <u>Thursday, August 23, 2012</u>		Sheet	<u>57</u> of <u>93</u>

PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	JMS0		3.1
Date: <i>Thursday, August 23, 2012</i>		Sheet	58 of 93

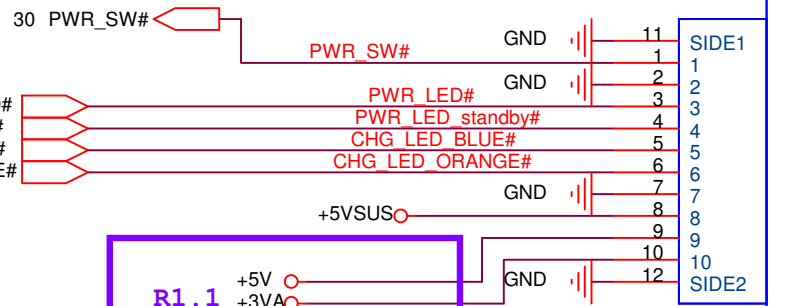


Power BTN and LED

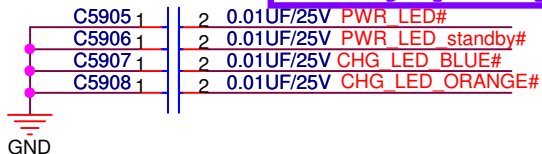
R2.0 12/19

R1.1
change for TP

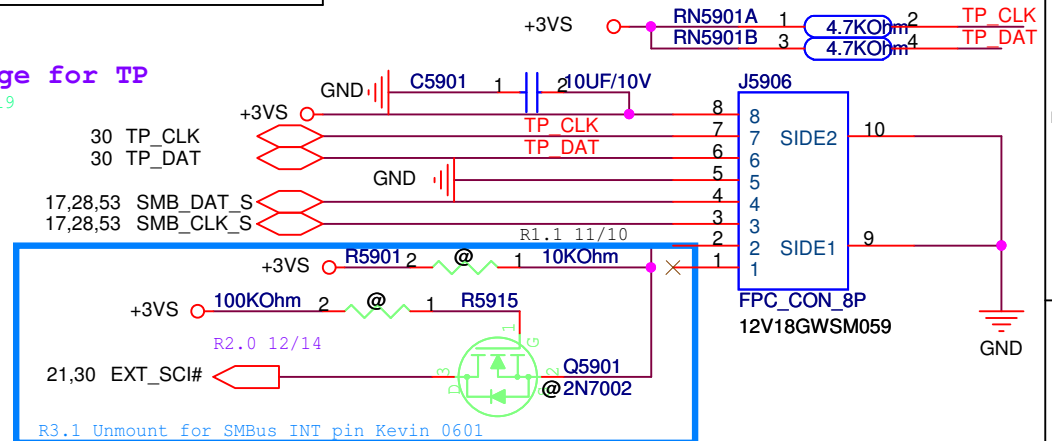
R2.0 12/19



R2.0 12/20

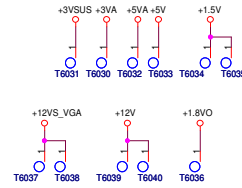
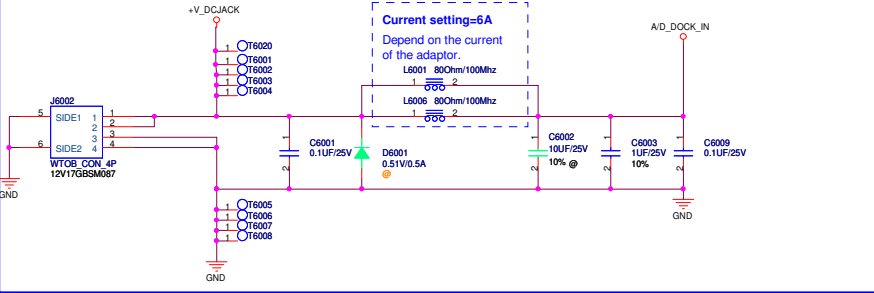


R2.0
change for Elan click pad



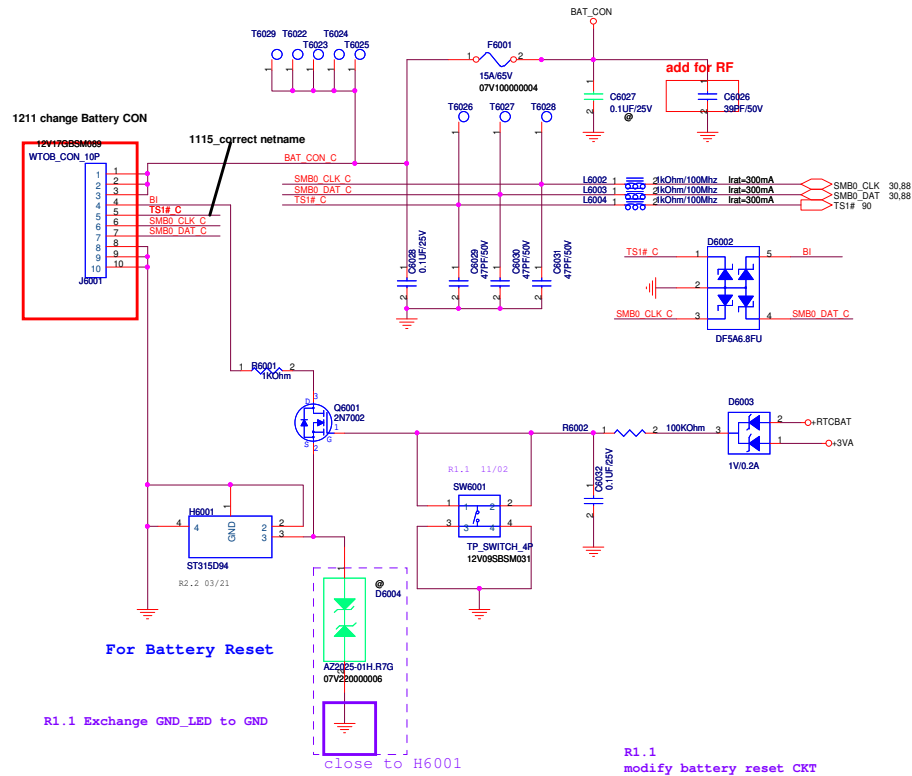
PEGATRON Title : B to B		
<OrgName>		Engineer: Joyoung Chianhg
Size A	Project Name JM50	Rev 3.1
Date: Thursday, August 23, 2012	Sheet 59	of 93

DC Jack WtoB CONN

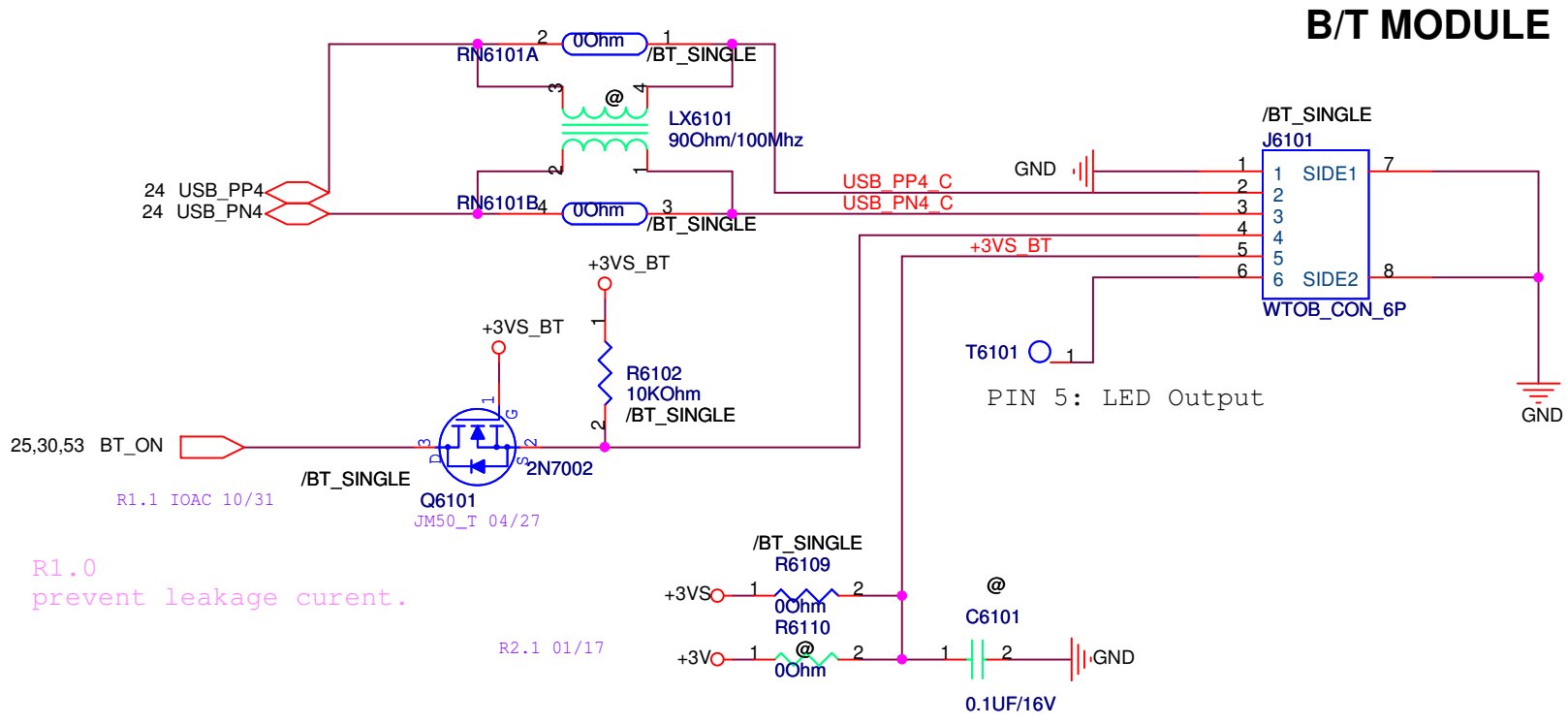


+VCC_RTC	+VCC_RTC	20,22,27
+3VA_EC	+3VA_EC	28,30,32
+3VA	+3VA	6,20,26,27,30,31,57,59,81,88,93
+5VA	+5VA	37,81,91
+3VSUS	+3VSUS	4,22,24,28,30,81,92
+5VSUS	+5VSUS	51,57,59,91
+12VSUS	+12VSUS	28,51,81,91
+1.5V	+1.5V	5,16,17,18,57,83
+3V	+3V	24,45,57,59,61,91
+5V	+5V	57,59,91
+12V	+12V	91
+0.75VS	+0.75VS	16,17,57,83
+1.05VS	+1.05VS	26,27,57,82,87
+1.5VS	+1.5VS	7,26,53,57,91
+1.8VS	+1.8VS	7,25,26,57,80,84
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+5VS	+5VS	27,31,36,37,45,48,50,51,57,80,87,91
+12VS	+12VS	28,36,48,91

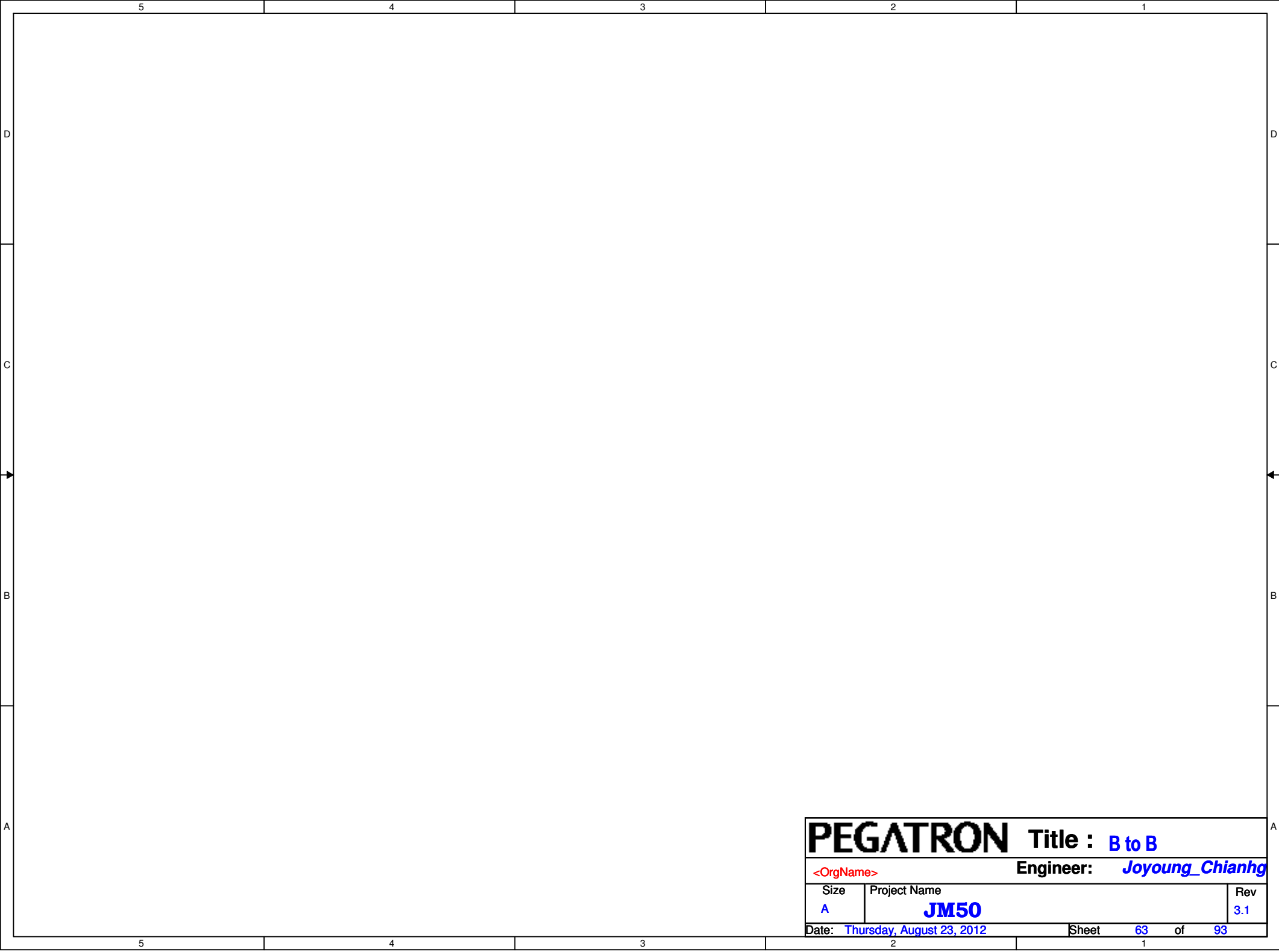
Battery Connector



AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
A/D_DOCK_IN	A/D_DOCK_IN	88
BAT_CON	BAT_CON	88
+VCCP	+VCCP	3,4,6,7,30,32,57,82
+VOCORE	+VOCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+VTT_PCH_ORG	+VTT_PCH_ORG	22,26,27
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,26,27
+V_VREF_DDR3	+V_VREF_DDR3	16,17,18

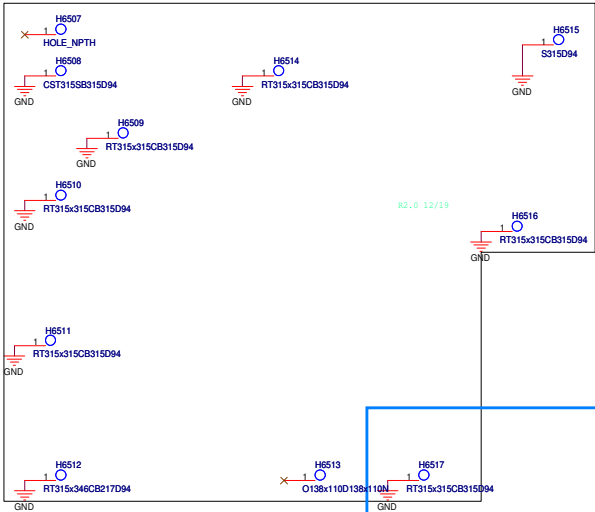
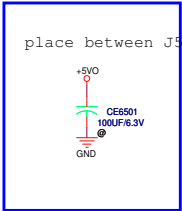
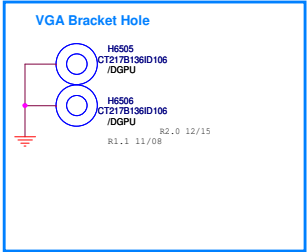
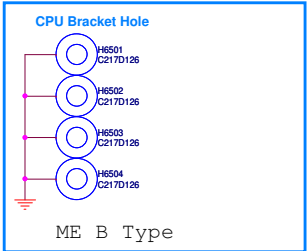


PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	JMS0		3.1
Date: <i>Thursday, August 23, 2012</i>		Sheet	62 of 93

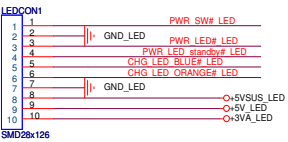


PEGATRON			Title : B to B		
<OrgName>			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
A	JM50				3.1
Date: Thursday, August 23, 2012			Sheet	63	of 93

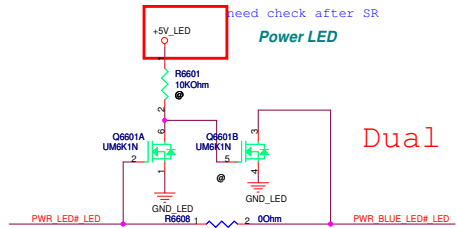
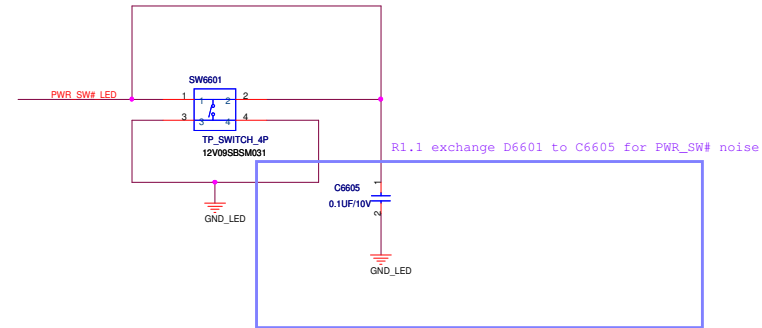




This screw hole should be Upside down(TOP and BOTTOM) .

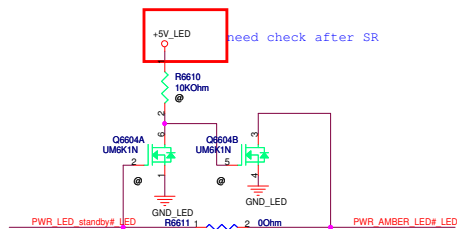


Power Button

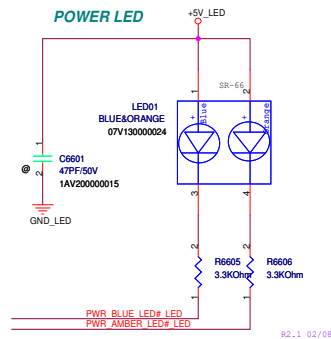


Power LED

Dual Color



need check after SR



POWER LED

LED01
BLUE&ORANGE
07V1300000024

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

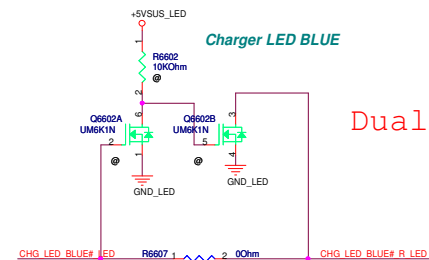
GND_LED

GND_LED

GND_LED

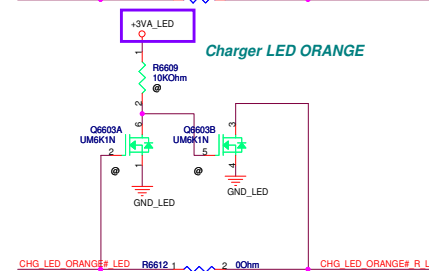
GND_LED

R2.1 02/08

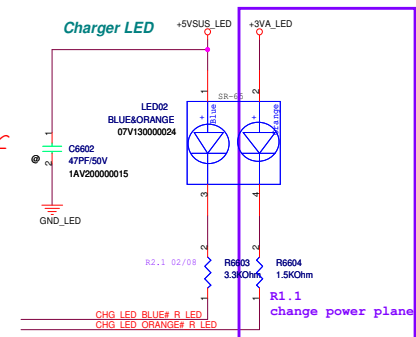


Charger LED BLUE

Dual Color



Charger LED ORANGE



Charger LED

LED02
BLUE&ORANGE
07V1300000024

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

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GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

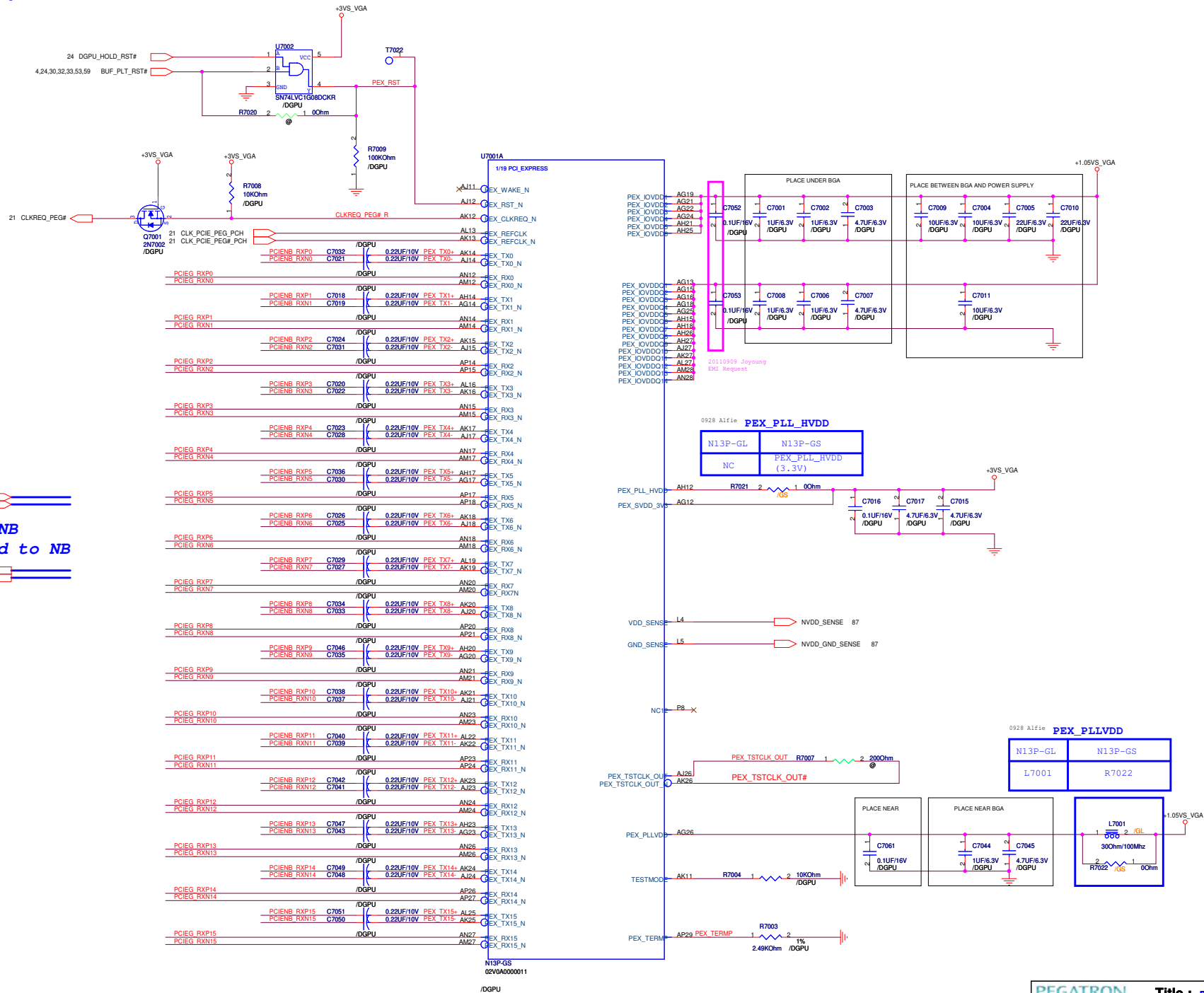
GND_LED

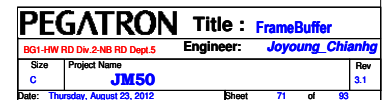
GND_LED

GND_LED

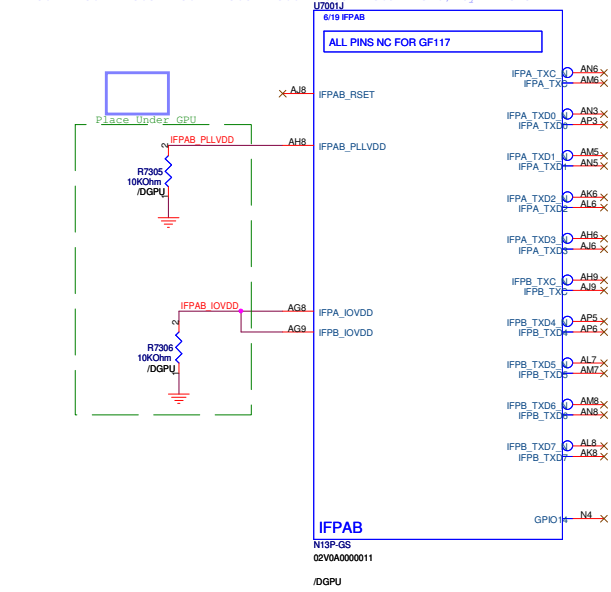
R1.1 change power plane

Frank
20110513 Change N13P GPU.

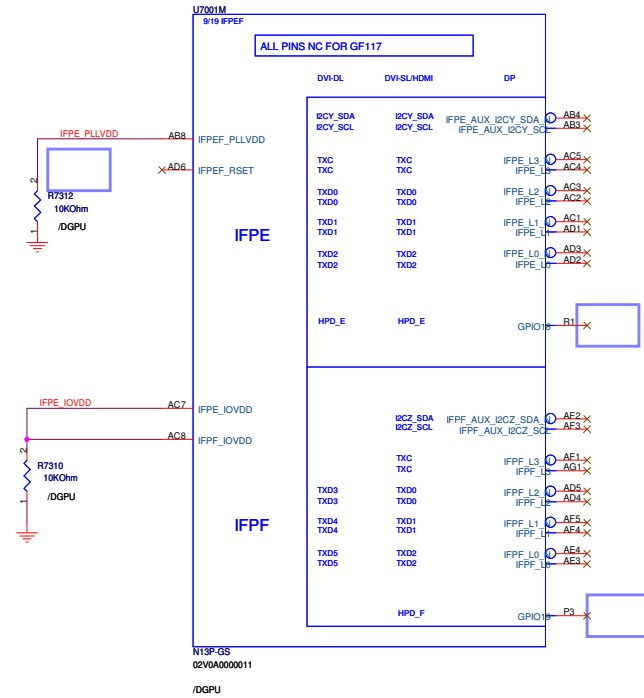
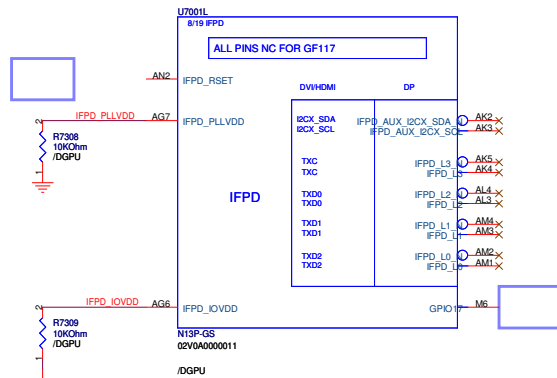
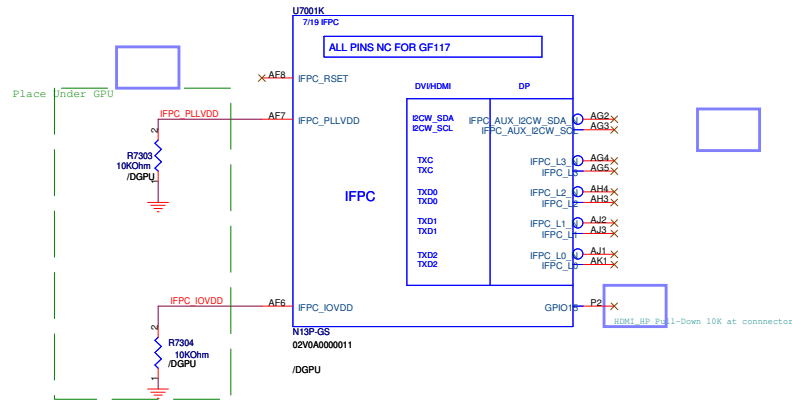


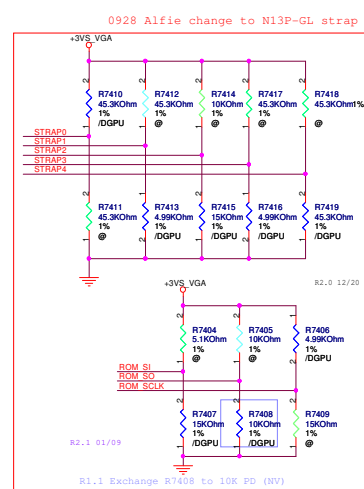


LVDS
R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7308 T7309 T7310) by Nvidia



HDMI





TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	V _I [3C]	GND [3C]
5K	1000 B	0000 B
10K	1001 9	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
40K	1111 F	0111 7

```

STRAP0
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/+
0 0 0 0 XGA -/+
0 0 0 0 SXGA +/+
0 0 0 0 SXGA +/+
0 0 0 0 HXGA +/+
0 0 0 0 HXGA +/+
1 1 1 1 SDR16 N/A

ROM_S1_RAMCONFIG
ROM_SIZE
Hynix 64Mx16 -> ram_cfg = 0x2
Samsung 64Mx16 -> ram_cfg = 0x3
Hynix 128Mx16 -> ram_cfg = 0x4
Samsung 128Mx16 -> ram_cfg = 0x7

ROM_S0
LOGICAL BIT
0 1 CLKM 417
1 2 F0 RAM_SIZE
0 3 SMD_A1T_ADDR
0 4 VGA_DEVICE

ROM_SCLK
LOGICAL BIT
3 2 PCI_DEVICE[4]
2 1 SUB_DEVICE
0 0 SLOTT_CLK_CFG
0 0 PLL_EXT_TERM

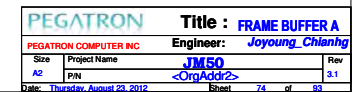
N1SP_GL

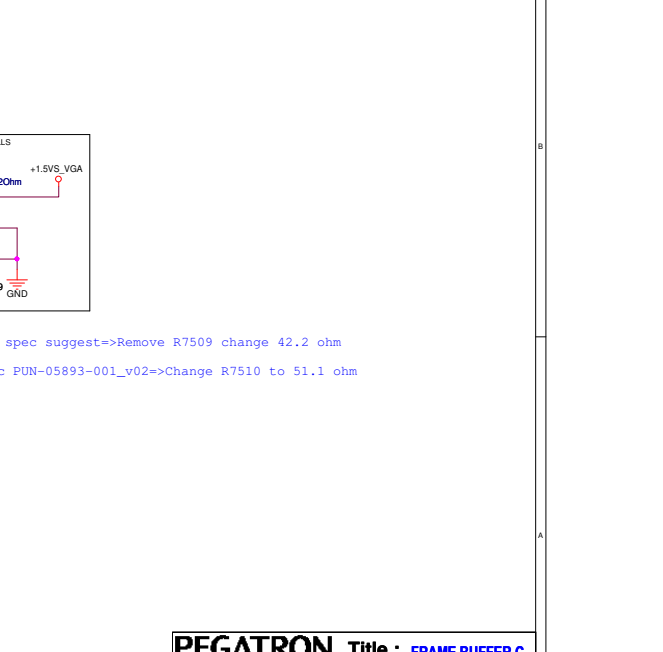
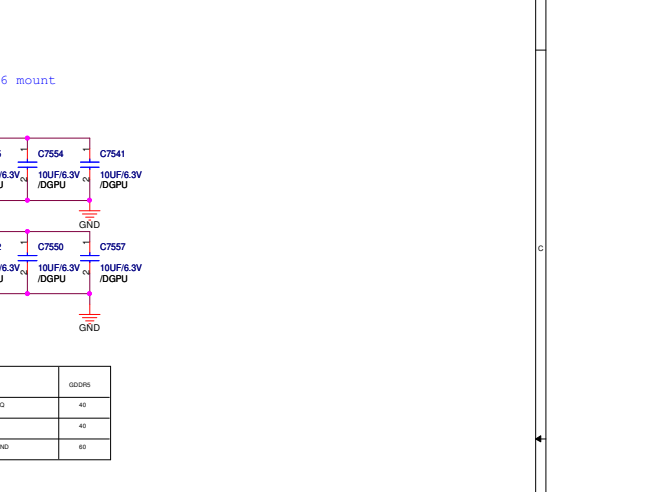
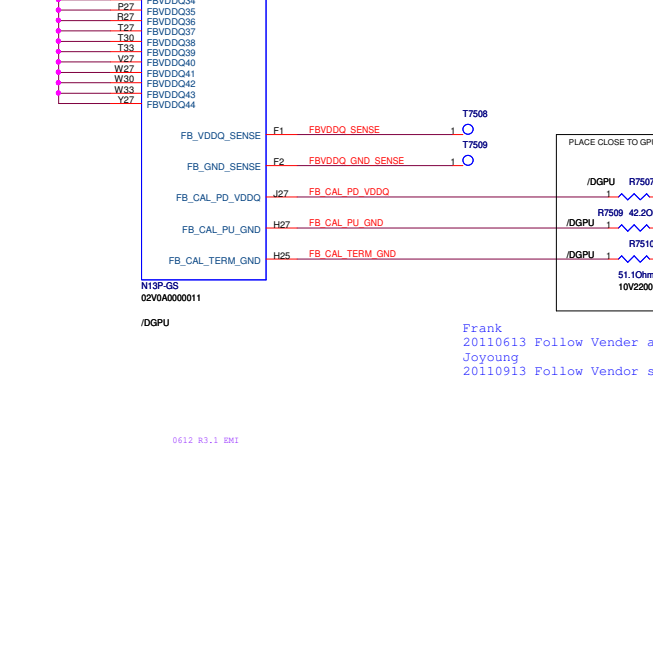
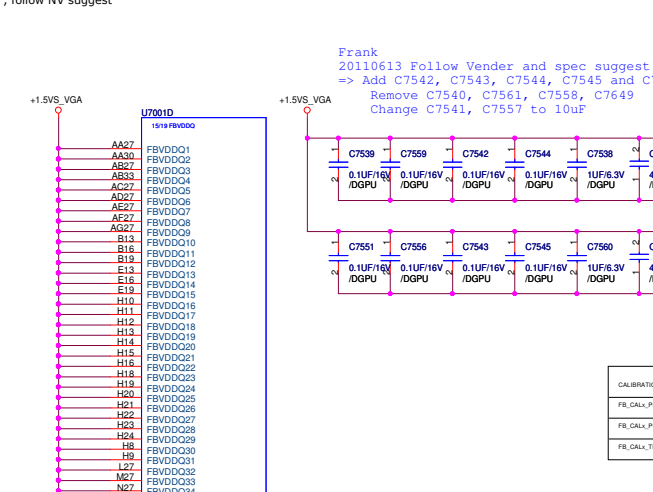
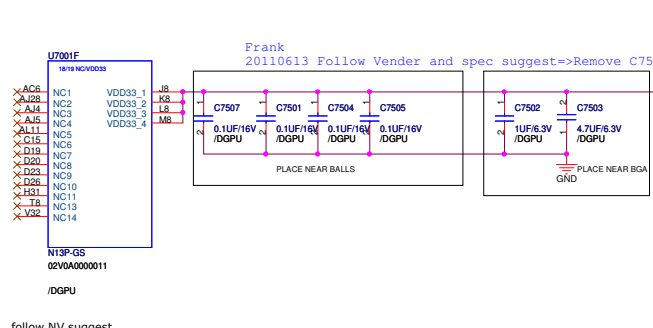
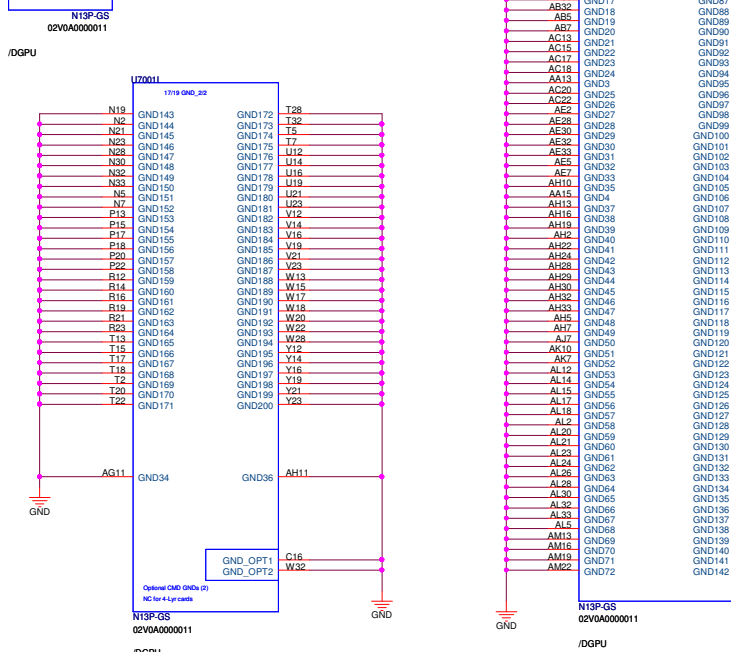
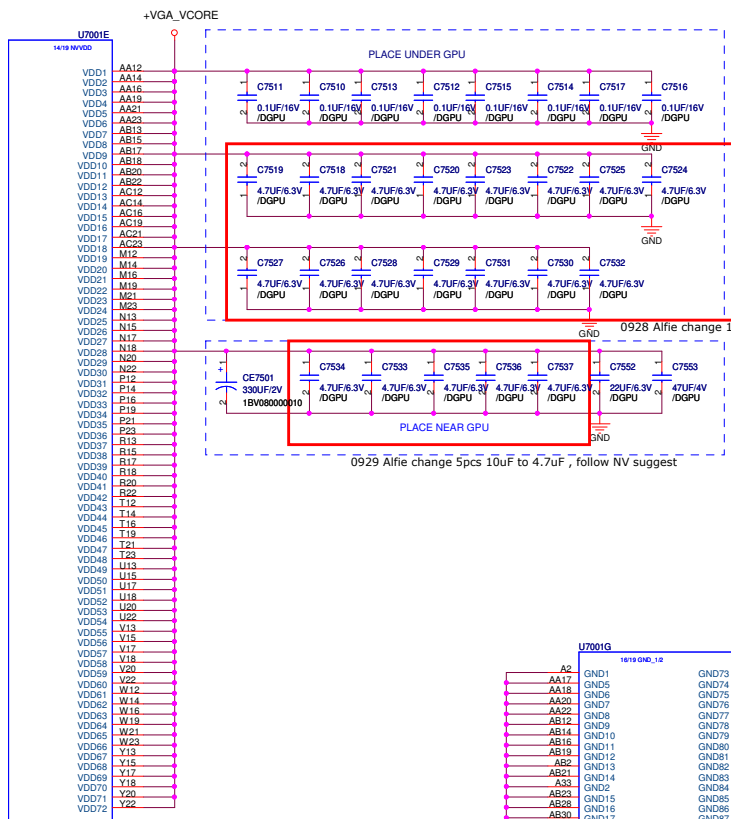
```

N13P-GL				
DEVICE ID	0xDE9			
STRAP0	45K PU	ROM1_SCLK	15K F	
STRAP1	45K PD	ROM1_SI	04x16	
STRAP2	10K FU		Hynix	15K PU
STRAP3	NC		128X16	
STRAP4	NC		Hynix	35K PU
		ROM1_SO		30K F

R1.1 Remove L_VDDEN_VGA & LCD_BKEN_VGA

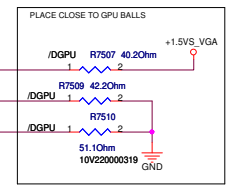
R1.1 Remove L_VDDEN_VGA & LCD_BKEN_VGA signals, No function request on the pin (NV)





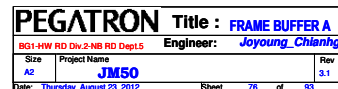
Frank
20110613 Follow Vender and spec suggest=>Remove C7506, C7508
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF

CALIBRATION PIN	QDQPS
FB_CALX_PD_VDDQ	40
FB_CALX_PLU_GND	40
FB_CALX_TERM_GND	80

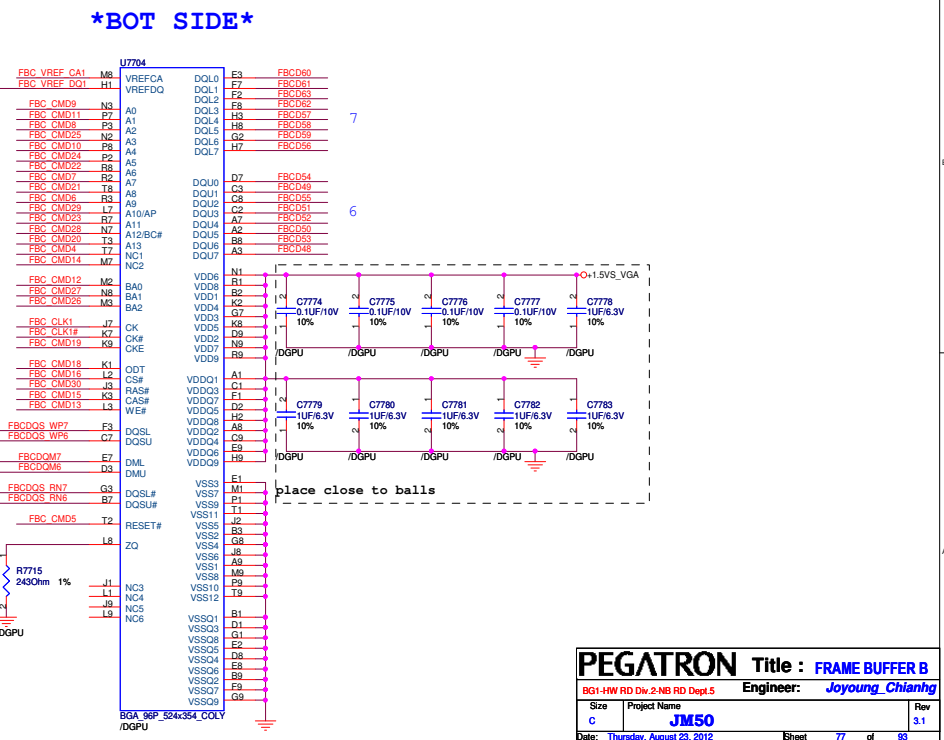
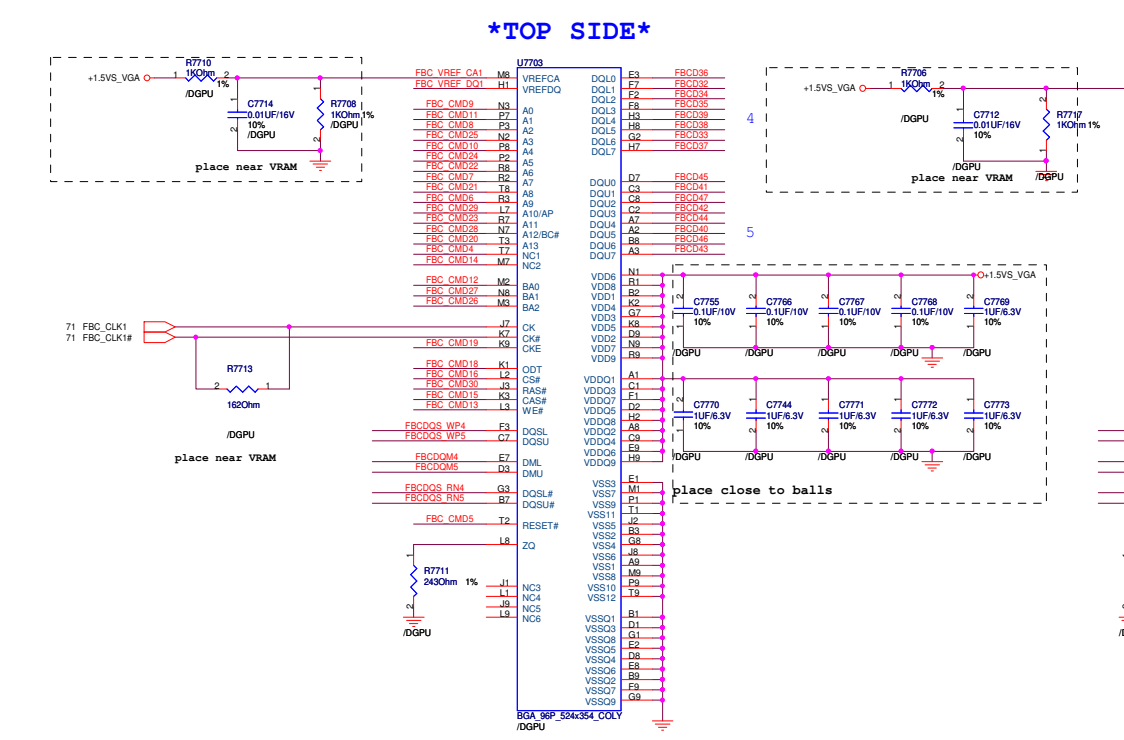
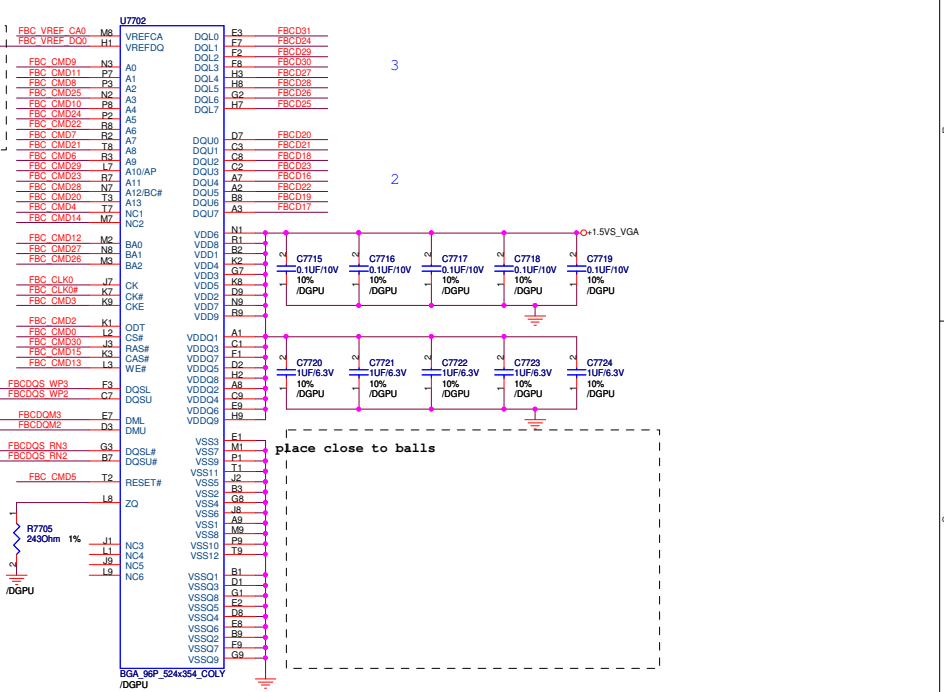
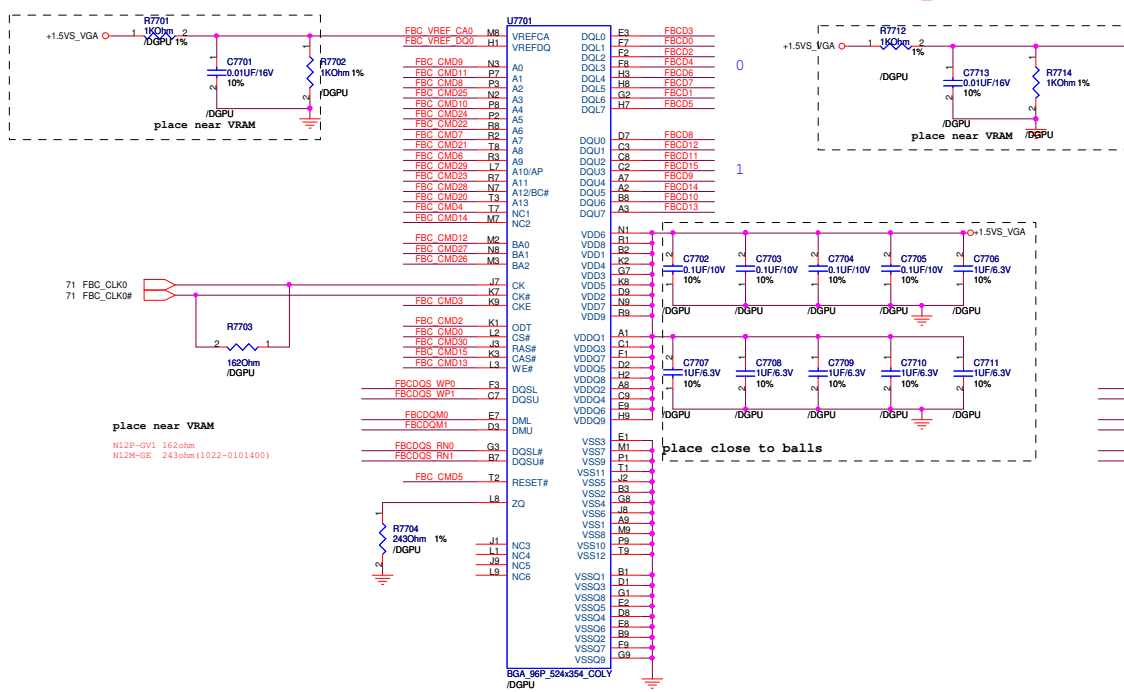


Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
Joyoung
20110913 Follow Vendor spec PUN-05893-001_v02=>Change R7510 to 51.1 ohm

TOP SIDE



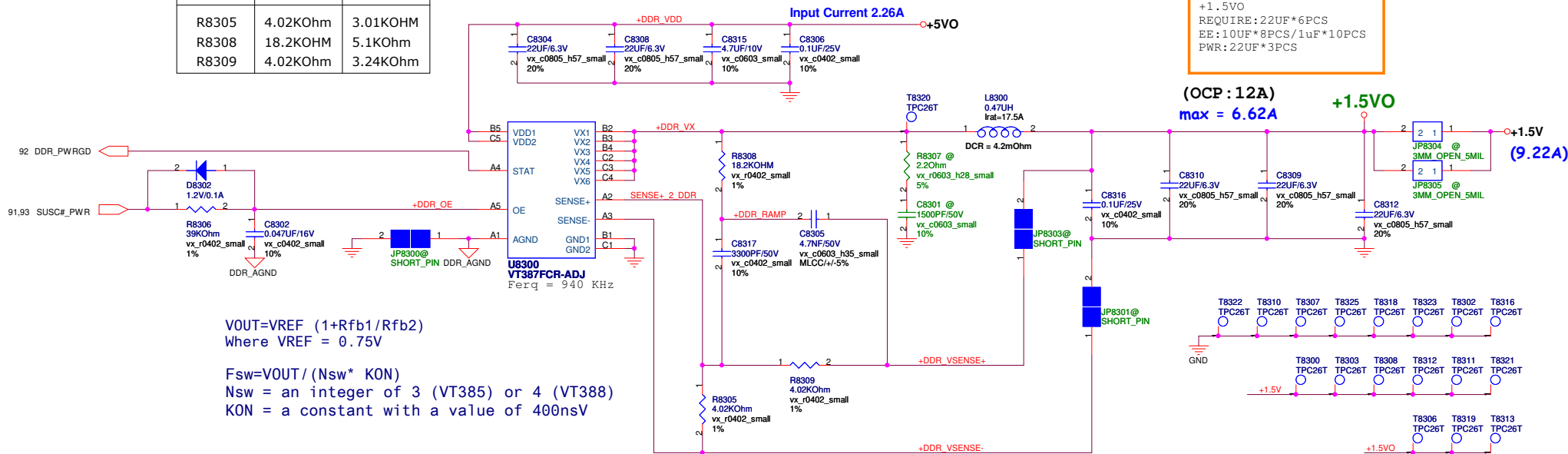
VRAM CH C



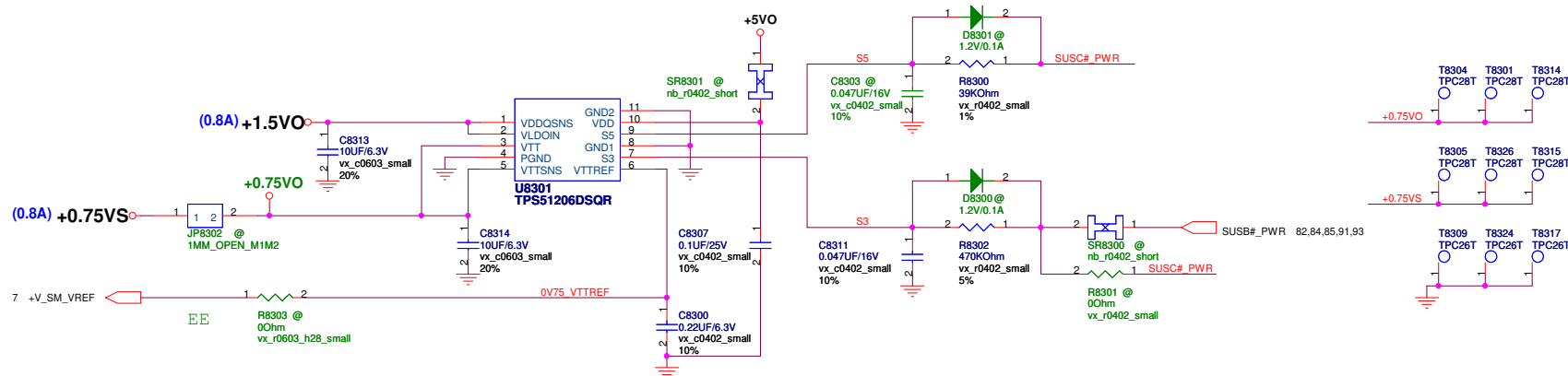
+1.5VO POWER SUPPLY

1.5VO	UMA	DSC
Vout	1.5V	1.557V
R8305	4.02KOhm	3.01KOhm
R8308	18.2KOhm	5.1KOhm
R8309	4.02KOhm	3.24KOhm

11/07/21
+1.5VO
REQUIRE: 22UF*6PCS
EE: 10UF*8PCS/1uF*10PCS
PWR: 22UF*3PCS



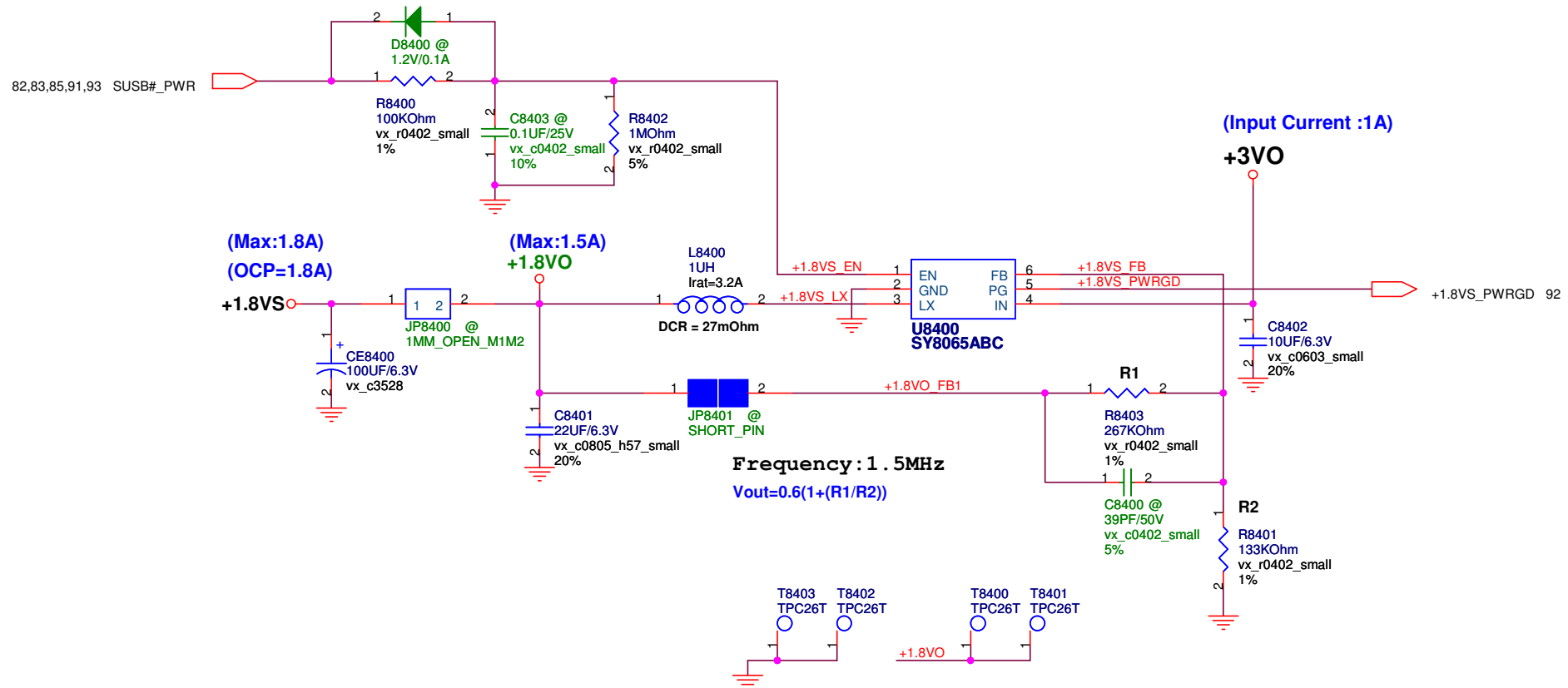
+0.75VS POWER SUPPLY



<Variant Name>

PEGATRON		Title :	POWER_DDR & VTT	
		Engineer:	Clark Liang	
Size Custom	Project Name JM50		Rev 1.0	
Date: Thursday, August 23, 2012		Sheet	83	of 94

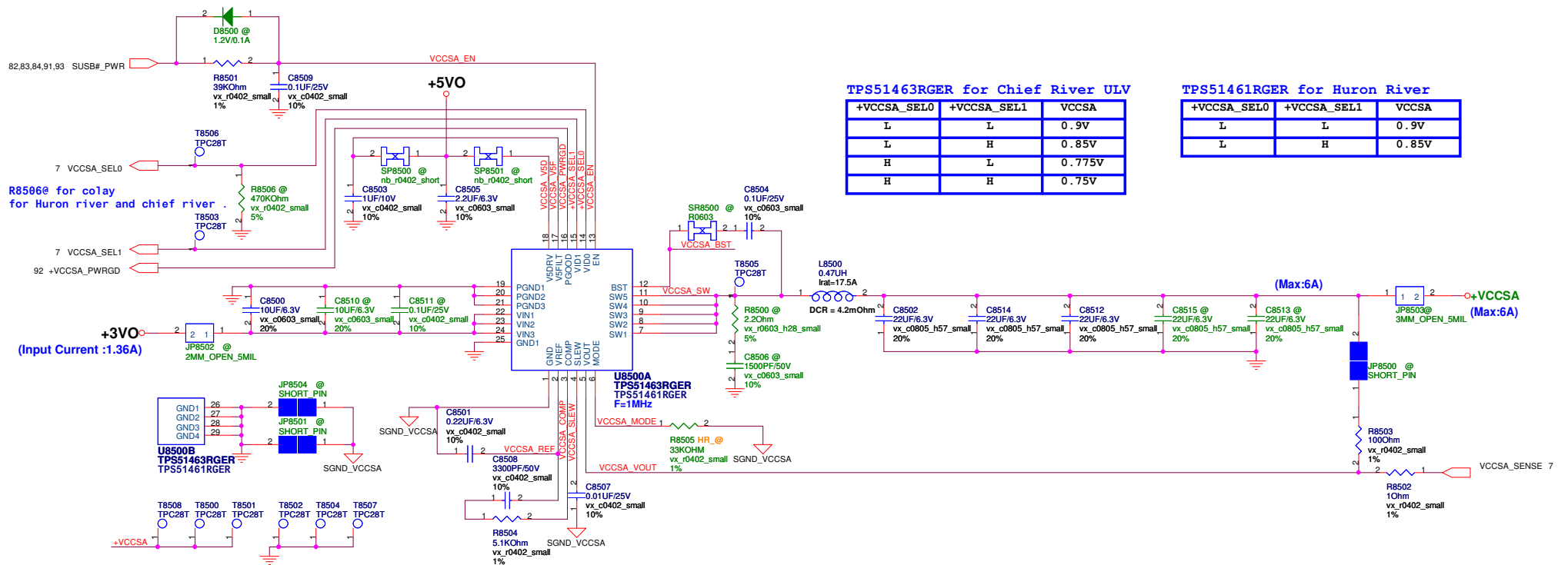
+1.8VS POWER SUPPLY



<Variant Name>

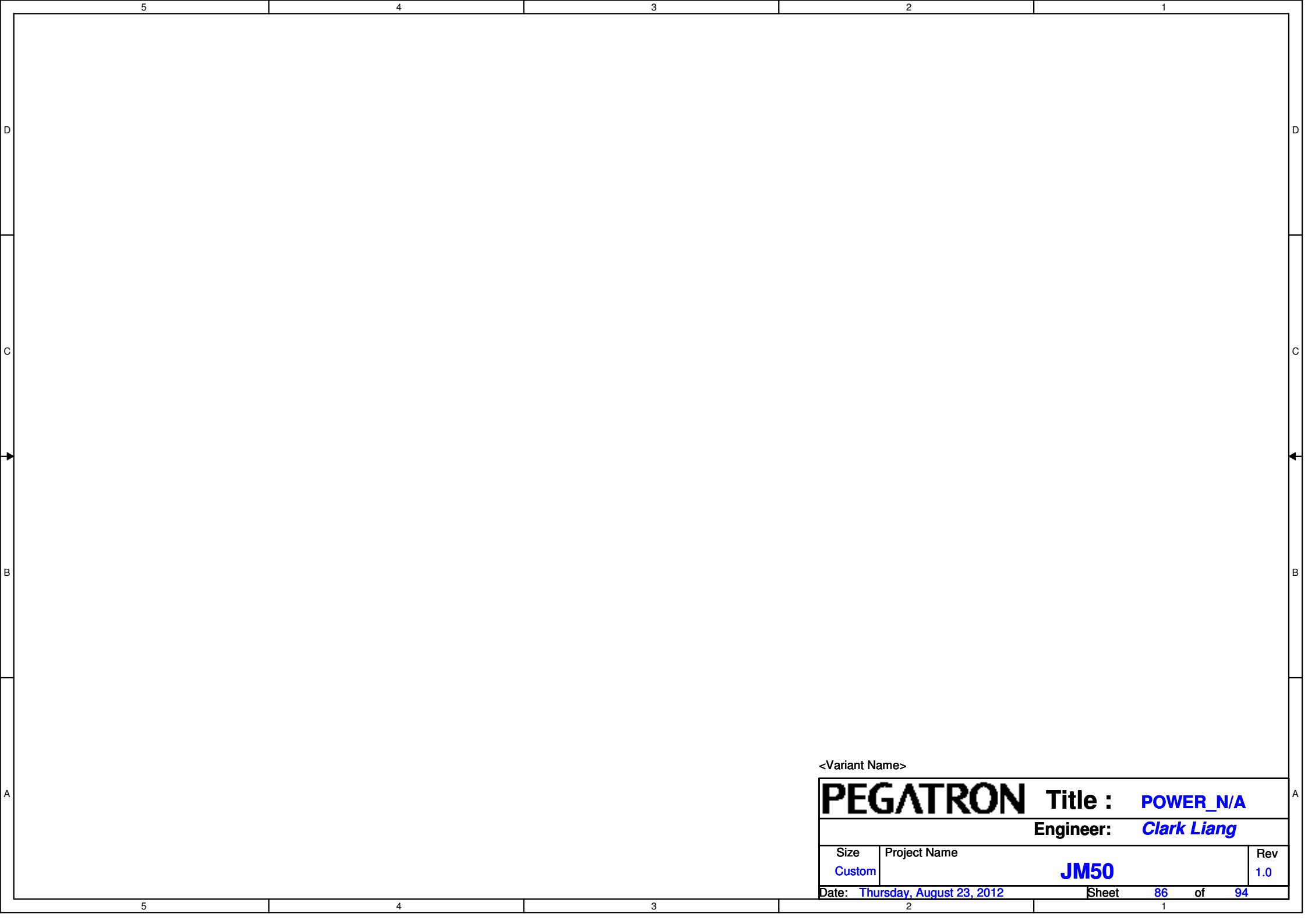
PEGATRON		Title :	POWER_+1.8VS
		Engineer:	Clark Liang
Size	Project Name	JM50	Rev
Custom			1.0
Date: Thursday, August 23, 2012		Sheet	84 of 94

VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

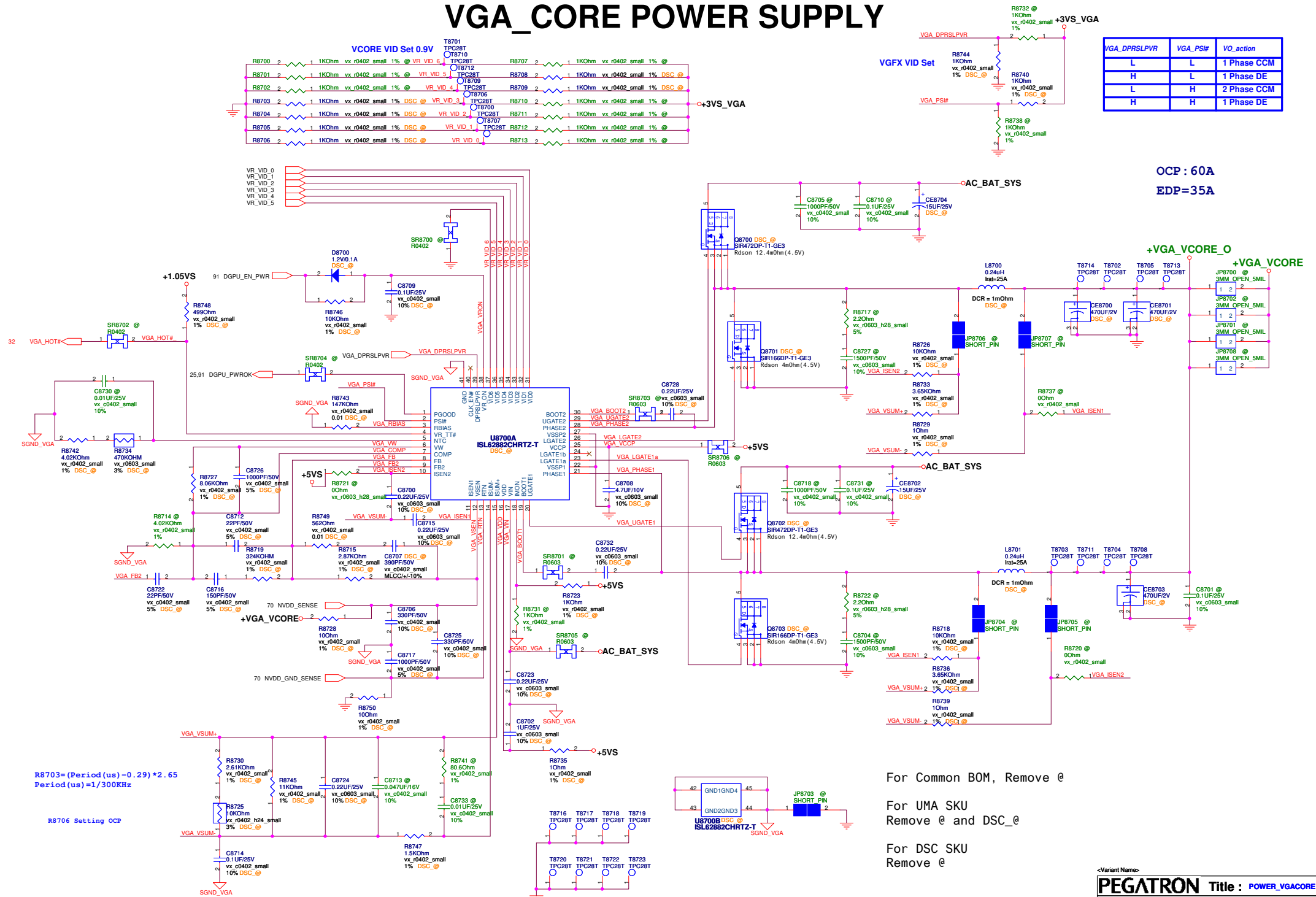
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V



<Variant Name>

PEGATRON		Title :	POWER_N/A
		Engineer:	Clark Liang
Size	Project Name		Rev
Custom	JM50		1.0
Date: Thursday, August 23, 2012		Sheet	86 of 94

VGA_CORE POWER SUPPLY



For Common BOM, Remove @

For UMA SKU
Remove @ and DSC_@

For DSC SKU
Remove @

<Variant Name>

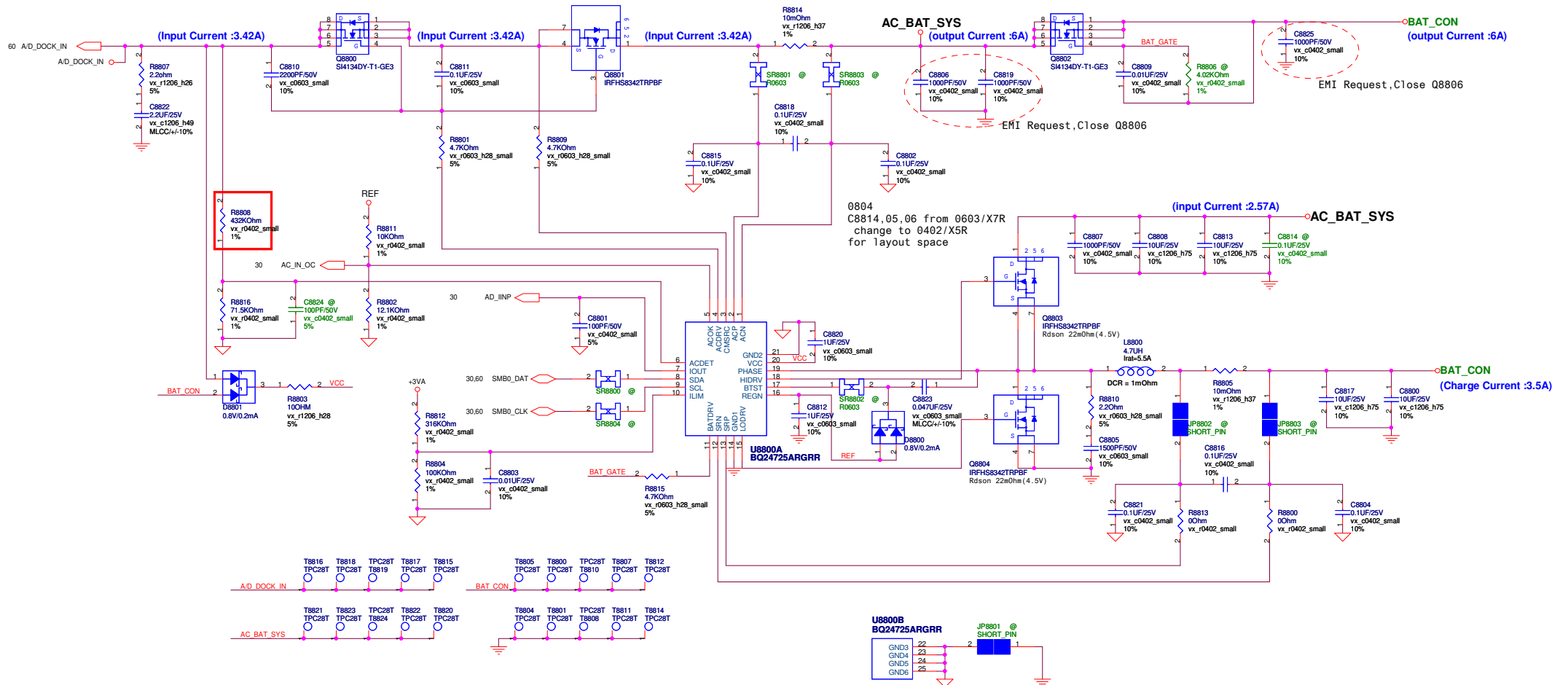
PEGATRON Title : POWER_VGACORE

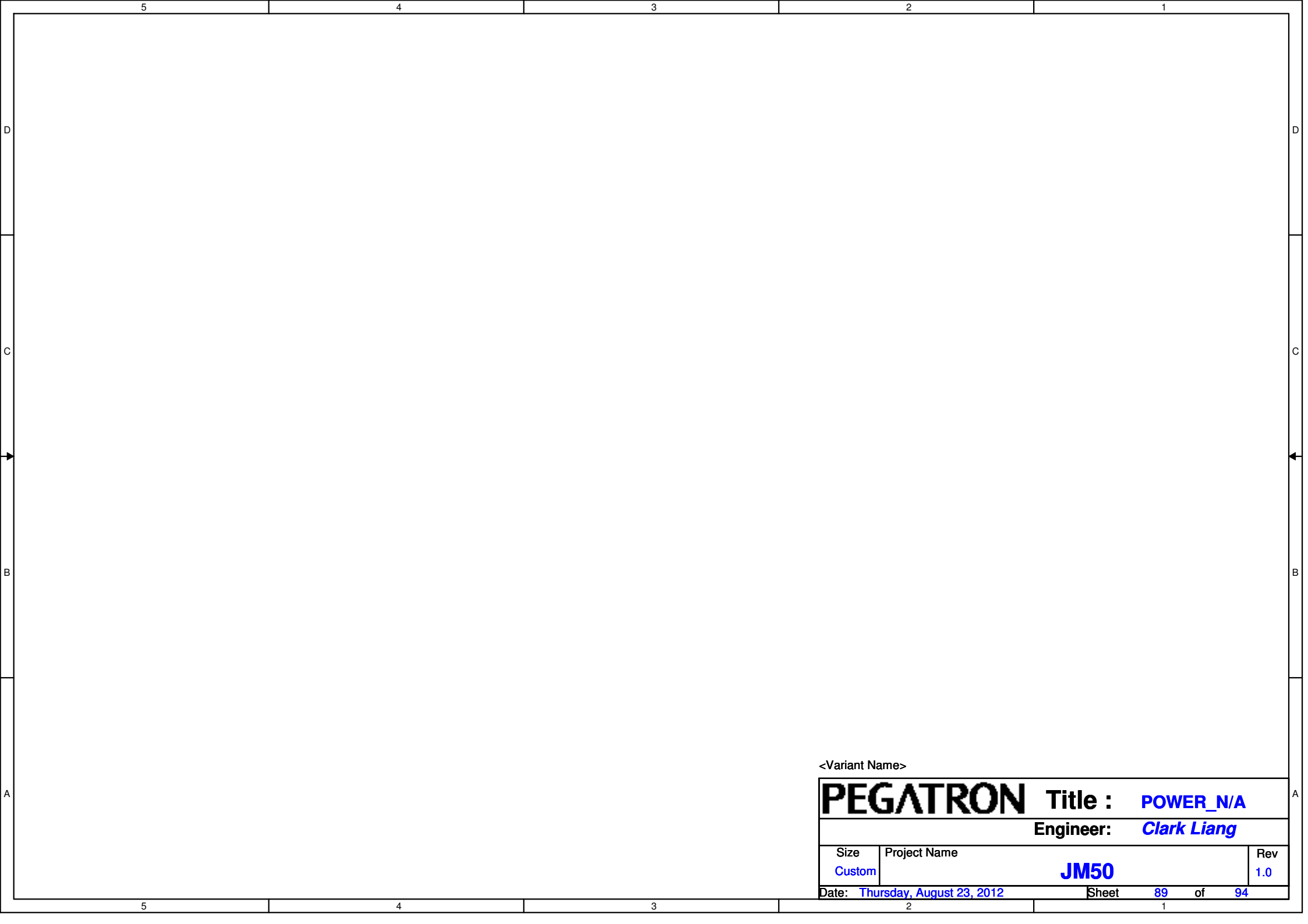
Engineer: **Clark Liang**

Size	Project Name	Rev
------	--------------	-----

Custom	JM50	1.0
Date: Thursday, August 23, 2012	Sheet 87 of 94	

BATTERY CHARGER





<Variant Name>

PEGATRON		Title :	POWER_N/A
		Engineer:	Clark Liang
Size	Project Name		Rev
Custom	JM50		1.0
Date: Thursday, August 23, 2012		Sheet	89 of 94

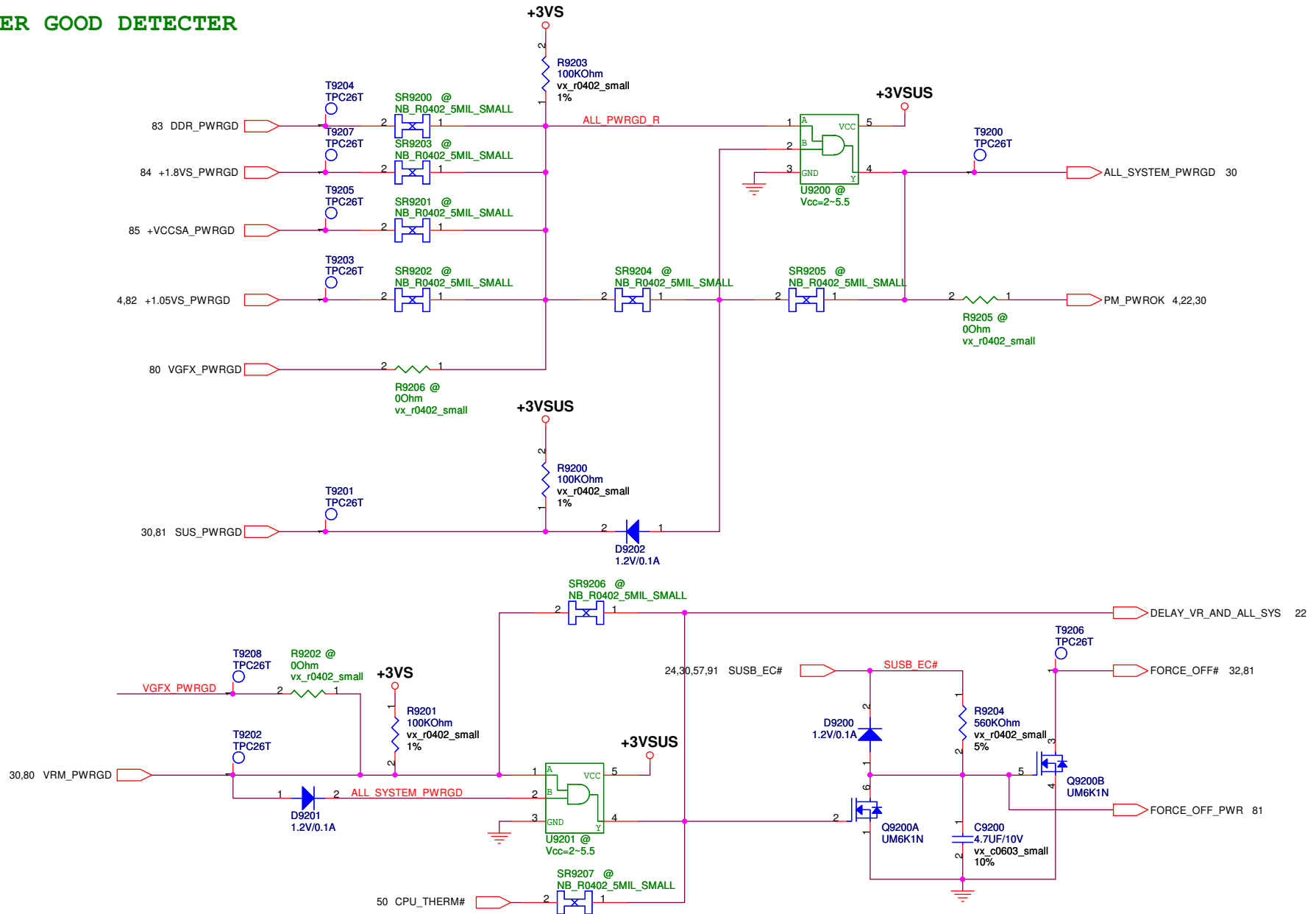
BATTERY IN DETECT



<Variant Name>

PEGATRON		Title : POWER_DETECT	
		Engineer: Clark Liang	
Size Custom	Project Name JM50		Rev 1.0
Date: Thursday, August 23, 2012		Sheet	90 of 94

POWER GOOD DETECTOR

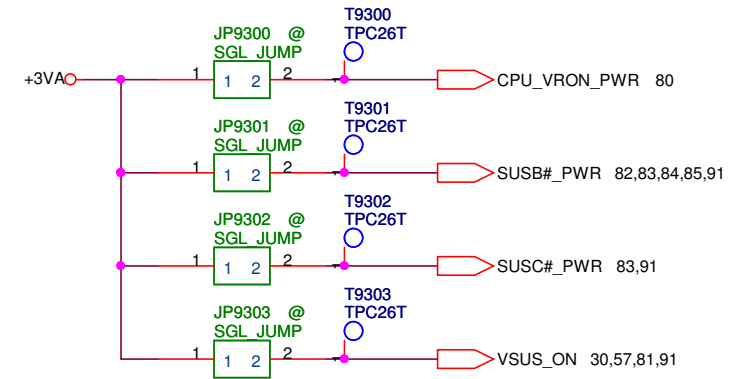


<Variant Name>

PEGATRON		Title : POWER_PROTECT	
		Engineer: Clark Liang	
Size Custom	Project Name JM50	Rev 1.0	
Date: Thursday, August 23, 2012		Sheet 92 of 94	

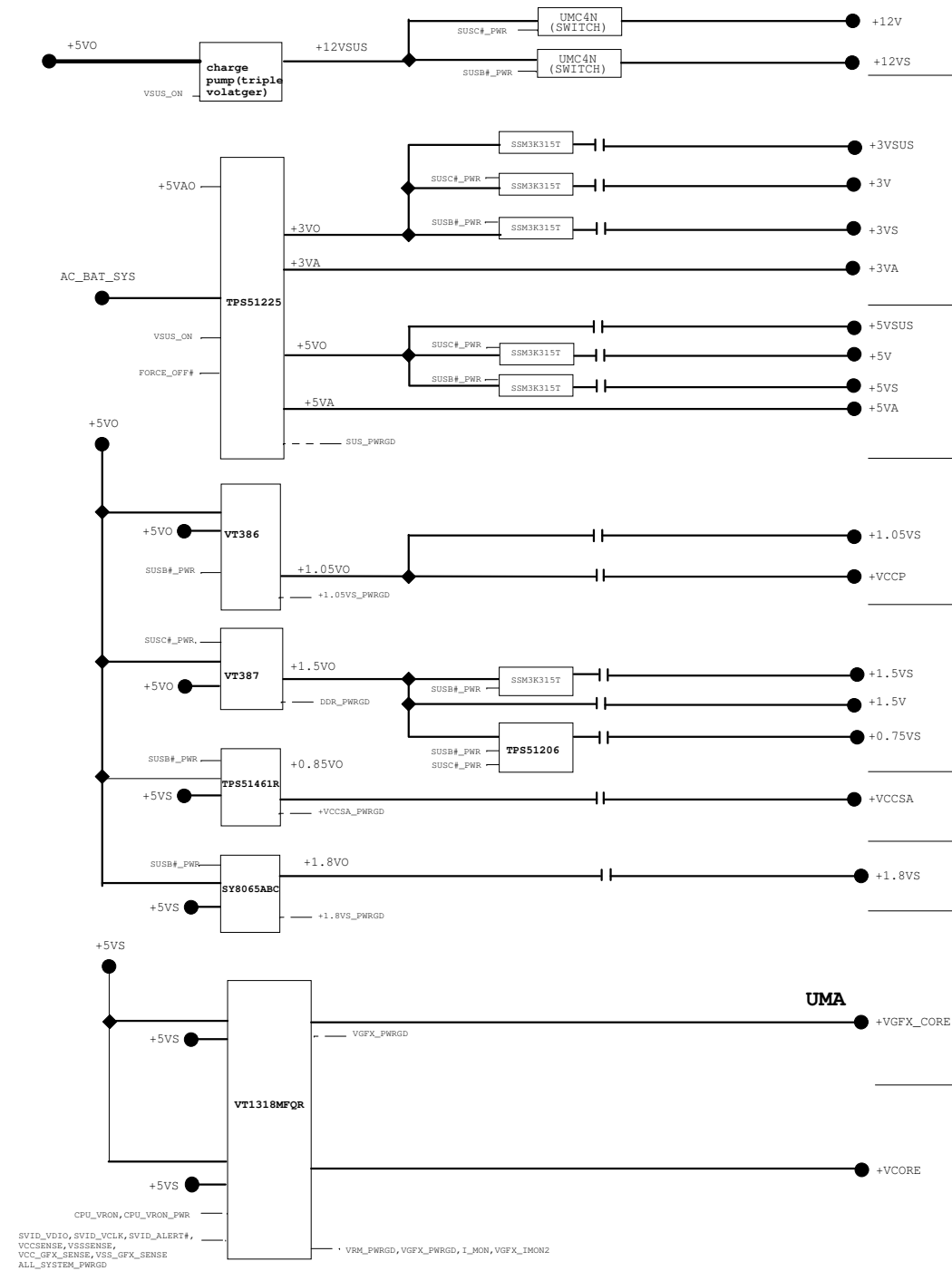
AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	37,60,81,91
+3VA	+3VA	6,20,26,27,30,31,57,59,60,81,88
+5VO	+5VO	52,65,80,81,82,83,85,91
+3VO	+3VO	53,81,84,85,91
+1.8VO	+1.8VO	60,84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	28,51,81,91
+5VSUS	+5VSUS	51,57,59,91
+3VSUS	+3VSUS	4,22,24,28,30,60,81,92
+12V	+12V	60,91
+5V	+5V	57,59,60,91
+3V	+3V	24,45,57,59,61,91
+1.5V	+1.5V	5,16,17,18,57,60,83
+12VS	+12VS	28,36,48,91
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS	+1.8VS	7,25,26,57,80,84
+1.5VS	+1.5VS	7,26,53,57,91
+1.05VS	+1.05VS	26,27,57,82,87
+VCCSA	+VCCSA	7,85
+0.75VS	+0.75VS	16,17,57,83
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+12VS_VGA	+12VS_VGA	60,91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Clark Liang	
Size	Project Name		Rev
Custom	JM50		1.0
Date: Thursday, August 23, 2012		Sheet	93 of 94



SPEC rating

(10mA)

(10mA)

(0.319A)

(0.278A)

(1.809A)

(0.07A)

(0.021A)

(1.615A)

(1.783A)

(0.1A)

(3.37A)

(5.95A)

(0.009A)

(9.688A)

(1A)

(4.8A)

(1.002A)

(12A)

(21.5A)

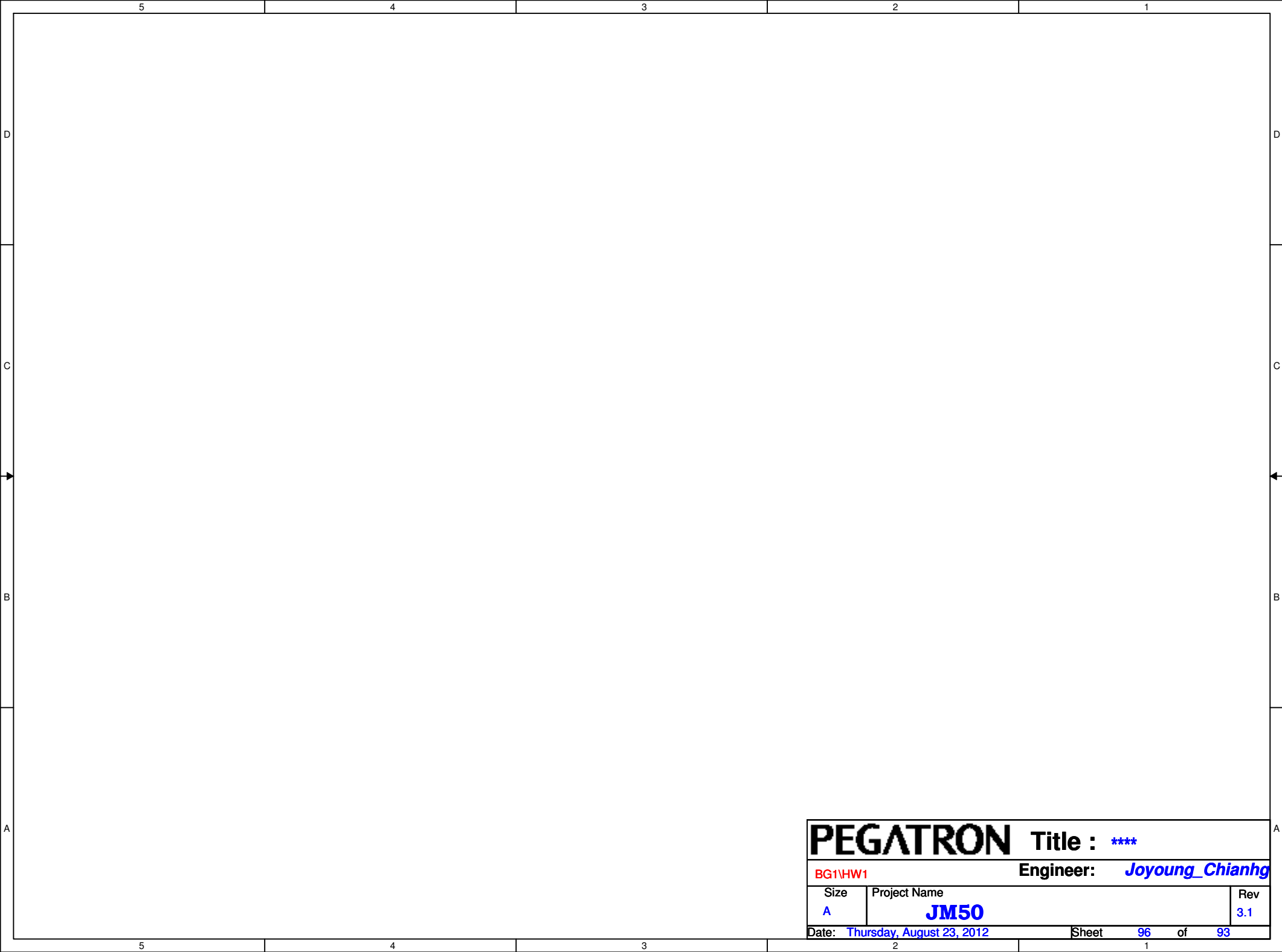
<Variant Name>

PEGATRON Title : **POWER_FLOWCHART**

Engineer: **Clark Liang**

Rev: **1.0**

Date: **Monday, August 25, 2014** Sheet: **04** of **04**



SR BOM change

- SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310
- SR1.2 CE5001 un-mount
- SR1.3 L3602 mount
- SR1.4 R7005 un-mount
- SR1.5 R7410 change 10K ohm
- SR1.6 R4504 change 10K ohm for LVDS backlight
- SR1.7 R7430, R7432, R7433 un-mount
- SR1.8 R7608, R7611 change 162 ohm

ER

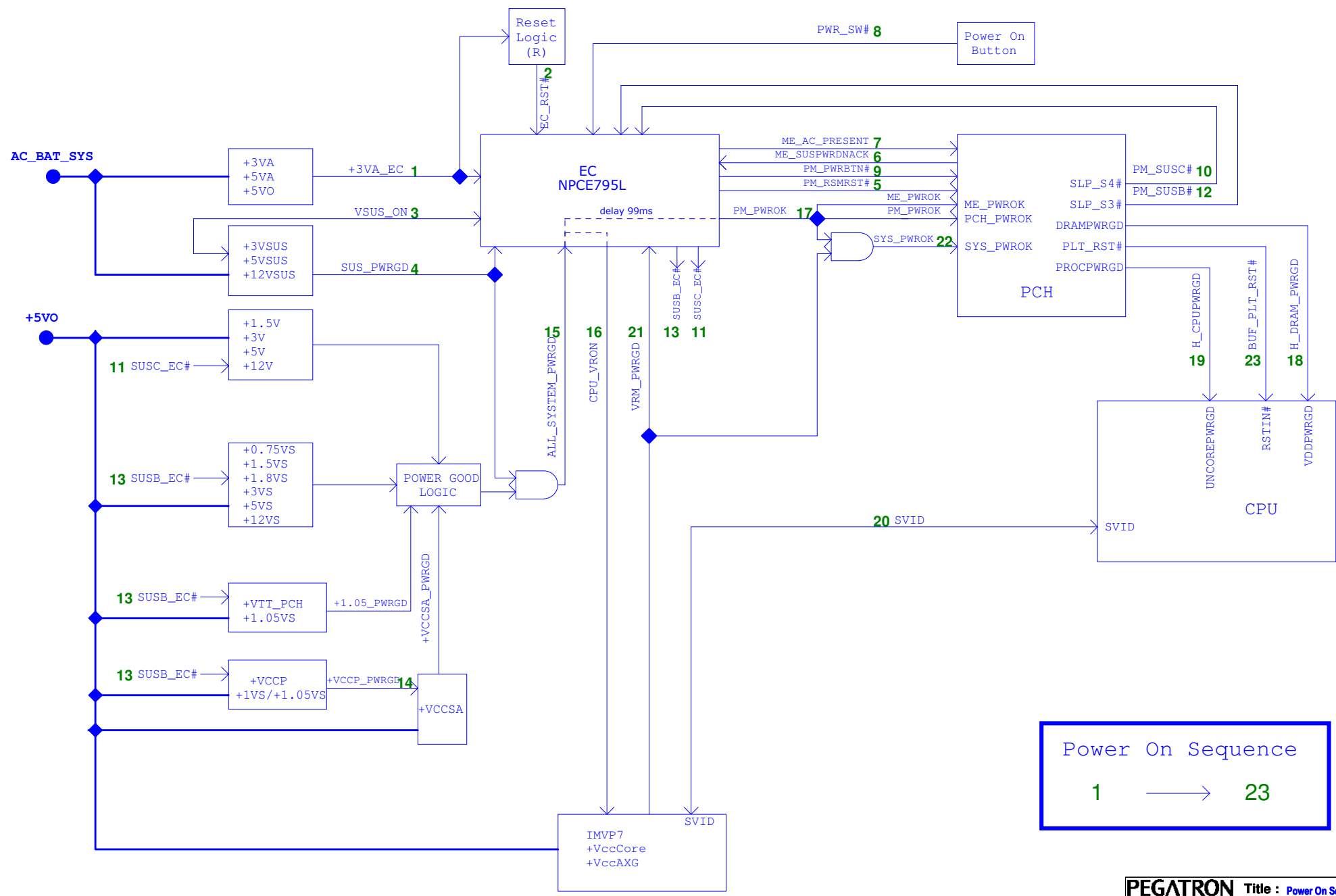
- ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
- ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
- ER1.3 U5201 change G547G1P81U for Desing IP
- ER1.4 Add Card Reader LED
- ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
- ER1.6 R6505~R6508 change 0603 size
- ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
- ER1.8 CPU_THERM# contact to FORCE_OFF#
- ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
- ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
- ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
- ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
- ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin, C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
- ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
- ER1.15 USB port 0 and port 1 swap
- ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
- ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
- ER1.18 reserve M_VREF schematic
- ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
- ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
- ER1.21 C6007, C6006 mount for WLAN
- ER1.22 RN3002 change 2R4P
- ER1.23 LED and BT schematic change to LED board
- ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
- ER1.25 VRAM change co-lay footprint
- ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
- ER1.27 Reserve C4516, C4517 to 10pF for RF request
- ER1.28 U6504,U6505 change AZ3028 for EMI request
- ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
- ER1.30 Add C6010 C6011 for EMI request
- ER1.31 Merge Q6704 and remove U6704
- ER1.32 D3720 change to mount for EMI request
- ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
- ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

- PR2.1 RTC pin define swap

- PR_S01:Change C3627,C3626 from X5R to Y5V
- PR_S02:According with INTEL datasheet suggest.(Power circuit mount)
- PR_S03:To prevent 誤動作 PCIE Wake.
- PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.
- PR_S05:To change 3G LED control by MODULE.
- PR_S06:To prevent leakage current and mount R for cost down.
- PR_S07:RF reserve.
- PR_S08:Move P.U 10K near 3G connector.
- PR_S09:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5VA_LEDDDB(+5VA) .(To resolve Battery LL issue)
- PR_S10:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5V_LEDDDB(+5V)
- PR_S11:Del JP, +3VS_CR change Net name to +3VS
- PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401
- PR_S13:Change NET name to +3VS
- PR_S14:Change 10uF to 22uF for wave of CRT display.
- PR_S15:Add 10uF (C6803)for USB droop test.
- PR_S16:D5201 PIN Swap
- PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944
- PR_S18:EMI add.
- PR_S19:Change to unmount for ME
- PR_S20:RF request.
- PR_S21:LED light fine-tune.
- PR_S22:BIOS request for UMA and DSC platform identifying.

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



Power On Sequence

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Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

